# Survey of Research Projects Conducted by Sasao's Group (FY2013-FY2020).

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***Abstract*—This paper surveys research projects conducted by Prof. Tsutomu Sasao's group from FY2013 to FY2020, at Meiji University. Research projects in this period can be divided into the following groups: 1) Index generation functions; 2) Classification functions; 3) Decomposition of functions; 4) Fast sequential circuits to evaluate decision diagrams; 5) Special circuits; 6) Decision diagrams; 7) History of logic design; 8) CAM optimization; 9) IC design tools; 10) Interconnection circuits; 11) EXOR logic synthesis; 12) Systems analysis using multi-valued decision diagrams; 13) Testable functions; 15) Miscellaneous Projects**

## I. Projects

### A. Index Generation Functions

An **index generation functions** is a mapping:

$$f : D \rightarrow \{1, 2, \ldots, k\},$$

where $D \subset B^n$, $B = \{0, 1\}$, $|D| = k$, that is $f$ is defined only for $k$ combinations,

Sasao conceived of the concept of index generation functions in 2008. It a mathematical model of a content addressable memory (CAM). CAMs are used for pattern matching, but they are expensive and dissipate high power. Sasao invented a circuit that performs the CAM operation using conventional memories and a small amount of glue logic. To implement index generation functions compactly, he developed various synthesis techniques [18], [42], [46], [60], [69], and [86].

### B. Classification Functions

A classification function is a generalization of an index generation function. It is useful for data-mining and machine learning. [89] considered hand-written character recognition. [87] showed a method to reduce the number of variables. [77] and [78] considered multi-valued input decision functions representing mushrooms, breast cancer and hepatitis. After moving to Meiji, Sasao shifted his research from logic design to data mining. This project has been selected as a JSPS grant for FY2020 to FY2022. Also, [78] was awarded a distinctive contributed paper award at ISMVL-2020.

### C. Decomposition of Functions

We considered three types of decompositions for index generation functions and classification functions.

**Functional Decomposition** can be implemented by the circuit shown in Fig. 1.1. Index generation functions with weight $k$ have a decomposition with $p \leq \lceil \log_2 k \rceil$, where $p$ denotes the number of connections between H and G.

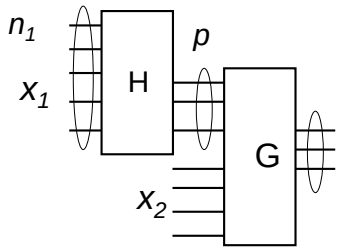


Fig. 1.1. Functional Decomposition

[52] shows an efficient method to find decompositions. A decomposition is **support-reducing** if $p < n_1$, where $n_1$ is the number of inputs for module $H$ in Fig. 1.1. [55] showed that support-reducing decomposition can be found efficiently for index generation functions. Note that for ordinary logic functions, detection of support-reducing decomposition is very hard. [50] and [63] used a Monte Carlo approach to predict the column multiplicity of decomposition charts for index generation functions.

**Linear Decomposition** can be implemented by the circuit shown in Fig. 1.2. When $k \ll 2^n$, **linear decompositions** are very effective. That is, index generation functions always have support-reducing disjoint decompositions. We assume that the cost of the linear part is $np$, while the cost of the general part is $m2^p$. Since $p$, the number of inputs to G is very important, we are interested in the size of $p$. By experimental results, we conjectured that $p \leq 2\lceil \log_2 k \rceil - 2$.

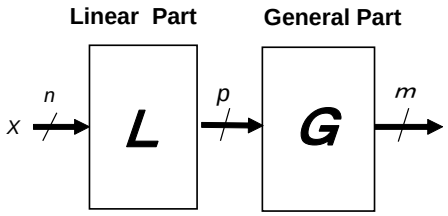


Fig. 1.2. Linear Decomposition

We analyzed bounds on $p$ [21], [24], [64], [68].

We developed various algorithms to reduce $p$, [2], [13], [15], [18], [28], [33], [36], [39], [48], [54], [56], [58], [61], [70], [76].

[90] considered a method to find an exact minimum linear decomposition for symmetric index generation functions. [85] considered irreducible index generation functions, for which no linear decomposition exist. [84] improved an upper bound on the number of variables $p$ to represent index generation functions using linear decompositions. Finally, it was proved that

$$p \leq \lceil 2 \log_2 k \rceil - 2.$$

[81] used dynamic programming to find an optimum linear decomposition for index generation functions.

**Row-shift Decomposition** is a new type of decomposition invented by Sasao in 2012. It uses an adder as shown in Fig.1.3. [7] considered cyclic row-shift decompositions. [65]

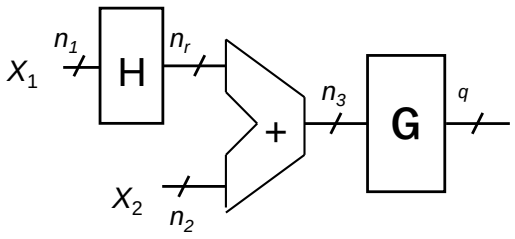


Fig. 1.3. Row-Shift Decomposition

and [80] analyzed the complexity of row-shift decompositions.

### D. Fast Sequential Circuits to Evaluate Decision Diagrams

To evaluate decision diagrams quickly, various sequential circuits were developed. This project was mainly conducted by Prof. Nakahara. [4], [9], [10], [11], [19], [20], [25], [31], [34], [43], [44], [57].

### E. Special Circuits

[41] and [73] used the Residue Number System (RNS) to implement neural networks. [32], [47] and [53] considered fast FFT circuits.

[6] considered various circuits to quickly generate functions having a certain property, including combinational number systems, permutations, and set partitions. [29] shows a circuit to generate partitions. [45] considered a set partition number system.

### F. Decision Diagrams

One of the most important problems in logic design is to represent logic functions compactly. Zero-suppressed decision diagrams (ZDDs) are such representations. We published an edited book on ZDDs [30].

### G. History of Logic Design

Sasao has been working with logic synthesis for more than 40 years. [1] analyzed highly cited papers on multi-valued logic (MVL). [5] surveyed Sasao's work on logic synthesis. [83] surveyed Sasao's work on EXOR logic synthesis. [75] described the first relay computer developed in Japan. Profs. Goto and Komamiya used various techniques to design an asynchronous relay computer, which is now displayed at the National Museum of Nature and Science, Tokyo, Japan. [37] summarized the work of Y. Komamiya on the design of arithmetic circuits using EXOR logic gates.

### H. CAM Optimization

A CAM is an important device for packet classification. Since CAMs are expensive and dissipate high power, they should be minimized. This project was related to I. Syafalni's Ph.D thesis.

CAM optimization: [8], [12], [14], [27].

CAM test: [38], [40], [51], [72], [74].

### I. IC Design Tool

This project was mainly conducted by Dr. I. Syafalni, who was working at a system design company in Fukuoka, Japan. The following papers are related to his work. [62], [67].

### J. Interconnection Network

With Prof. Y. Koga, Sasao developed a design method for multi-terminal universal interconnection networks [88].

### K. EXOR Logic Synthesis

In [71], a design method for multi-output linear circuits is shown. Such circuits are useful in the realization of the linear part of Fig. 1.2. In [59] and [66], methods to identify affine equivalence classes of logic functions are shown. Note that if two functions $f_1$ and $f_2$ are affine equivalent, then the two functions can be realized by the same circuit in Fig. 1.2, where $G$ is the same for $f_1$ and $f_2$.

### L. System Analysis using Multi-valued Decision Diagrams

This project was mainly conducted by Prof. S. Nagayama. [3], [16], [22], [26], [35].

### M. Testable Functions

Consider the class of single-output two-level irredundant AND-OR circuits. Inadmissible classes of functions cannot be caused by stuck-at faults [23], [49]. This project was mainly conducted by Prof. D. K. Das.

### N. Miscellaneous Projects

In addition to the other projects, Sasao performed miscellaneous projects with other researchers:

In [79] and [82], asymmetric logic functions are enumerated. In [91], properties of partition functions are analyzed. In [17], a method to design a numerical function generator is shown.

## II. Research Grants

During the period from FY2013 to FY2019, Sasao obtained the following grants:

**KAKEN (JSPS)**

- "Logic synthesis using linear transformation and memory," (April 2011 to March 2014).
- "Study on the design of fast updatable index generation circuits," (April 2014 to March 2017).
- "Study on decomposition of index generation functions," (April 2017 to March 2020).
- "Study on minimization of variables for classification functions, and their applications," (April 2020 to March 2023).

**A-STEP (JST)**

- "Low-power programmable logic circuits for pattern matching," (April 2013 to March 2014).

## III. Books

During this period, Sasao published two books: One is an edited book related to the Reed-Muller Workshop by Sasao and Butler in 2013. The other is a monograph on index generation functions.

- T. Sasao and J. T. Butler, *Applications of Zero-Suppressed Decision Diagrams*, Synthesis Lectures on Digital Circuits and Systems, Morgan-Claypool, November 2014, 123 pages.
- T. Sasao, *Index Generation Functions*, Synthesis Lectures on Digital Circuits and Systems, Morgan-Claypool, Oct. 2019, 184 pages.

## IV. Patent

During the period, Sasao obtained one international patent with the financial support of JST. Title: Content addressable memory, an index generator, and a registered information update method
Patent number: US9865350
Filed: August 19, 2015
Date of Patent: January 9, 2018
Assignee: Meiji University
Inventor: Tsutomu Sasao

## V. Awards

Sasao's group received many international awards. Major awards include:

1) **Outstanding Contributed Paper Award**, (awarded at ISMVL-2013).
   S. Nagayama, T. Sasao, and J. T. Butler, "Analysis of multi-state systems with multi-state components using EVMDDs," *International Symposium on Multiple-Valued Logic* (ISMVL-2012), Victoria, Canada, May 14-16, 2012, pp. 122-127.
2) **Best Paper Award**,(awarded at MCSoc-13).
   H. Nakahara, T. Sasao, and M. Matsuura, "A packet classifier using parallel EVMDD(k) machine," *7th IEEE International Symposium on Embedded Multicore SoCs* (MCSoC-13), Tokyo, Japan, Sept. 26-28, 2013.
3) **Outstanding Paper Award**, (awarded at SASIMI 2013).
   T. Sasao, Y. Urano, and Y. Iguchi,"A heuristic method to find linear decompositions for incompletely specified index generation functions," *The 18th workshop on Synthesis and System Integration of Mixed Information Technologies* (SASIMI-2013), Sapporo, Japan, Oct. 21-22, 2013, R3-1, pp. 143-148.
4) **Best Paper Award**,(awarded at IEEE TENCON 2017.)
   I. Syafalni, K. Wakasugi, and T. Sasao, "Probe location checker for IC physical verification," *2017 IEEE TENCON*, Penang, Malaysia, Nov. 5-8, 2017.
5) **Outstanding Contributed Paper Award**, (awarded at ISMVL-2019).
   S. Nagayama, T. Sasao and J. T. Butler, "An exact optimization method using ZDDs for linear decomposition of index generation function," ISMVL-2018, May 16-18, 2018, Linz, Austria.
6) **Distinctive Contributed Paper Award**, (awarded at ISMVL-2020).
   T. Sasao, "On a minimization of variables to represent sparse multi-valued input decision functions," *International Symposium on Multiple-Valued Logic*, (ISMVL-2019), May 21-23, 2019, Fredericton, Canada, pp. 182-187,

## VI. People

Many people involved in the projects: J. T. Butler (visiting researcher); H. Nakahara (Prof. Tokyo Institute of Technology); S. Nagayama (Prof. Hiroshima City University); Y. Iguchi (Prof. Meiji University); A. Mishchenko (Visiting researcher); I. Syafalni (Former Ph.D. student at Kyushu Institute of Technology, now a lecturer at Bandung Institute of Technology, Indonesia) .

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