Survey of Research Projects Conducted by Sasao's Group (FY2004-FY2011).

Tsutomu Sasao
Department of Computer Science and Electronics,
Kyushu Institute of Technology,
Iizuka 820-8502, Japan
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***Abstract*—This paper surveys research projects conducted by Prof. Tsutomu Sasao's group during FY2004 to FY2011. The research projects in this period can be divided into the following groups: 1) Cascade realizations; 2) Index generation functions; 3) Pattern matching circuits; 4) Decision diagrams; 5) Branching program machines; 6) Numerical function generators; 7) Classification functions; 8) Code converters; 9) FPGA designs; 10) Complexity measures for logic functions; 11) Functional decompositions; 12) Reconfigurable logic; 13) Spectral analysis of logic functions; 14) Boolean matching; and 15) Miscellaneous Projects**

I. Projects

A. Cascade Realization

Like the programmable logic array (PLA), a cascade has a regular structure, and is easier to design than random logic networks. Sasao found an efficient method to map a logic function represented by a binary decision diagram (BDD) into a cascade of lookup tables (or LUT cascade). He also invented a method to realize multiple-output logic function using a large (LUT) and a sequencer [9], [11], [13], [17], [19], [30], [31], [29], [35], [37], [48], [49], [41], [53], [65], [67], [82].

B. Index Generation Function

The most difficult task of the project was to find *killer* applications of LUT cascades. For this purpose, Sasao worked with Yamaha Corporation. An engineer of Yamaha suggested to apply it as an *address generator* in computer networks. This was the seminal idea in the project. From this, Sasao formulated the concept of **index generation functions** [38], [40], [43], [46], [47], [62], [63], [72], [76], [80], [84], [85], [97], [100], [102], [103], [108], [111], [112]. Afterwards, a cooperative project with Renesas Electronics Corporation was conducted.

C. Pattern Matching Circuits

In the second stage of the CLUSTER project (FY2007-FY2012), Sasao developed fast pattern matching circuits. It is a good application of LUT cascades developed in the first stage (FY2002 to FY2007). With H. Nakahara, Sasao developed exact matching and regular expression matching circuits [53], [78], [80], [86], [98], [101], [104], [116], [121]. Major applications of index generation function include: address tables in the internet, terminal access controllers, memory patches, code converters, scanning engines for computer virus, DNA matching, and text compressions.

D. Decision Diagrams

One of the most important problems in logic synthesis is to represent logic functions compactly while maintaining low delay. Binary decision diagrams (BDDs) are such representations. With S. Nagayama, Sasao considered various decision diagrams to represent logic functions: Multi-valued decision diagrams (MDDs), and heterogeneous MDD [10], [6], [4], [8].

E. Branching Program Machines

Branching program machines are circuits that evaluate logic function represented by decision diagrams. Sasao investigated a circuit that evaluates each type of decision diagram. The advantage of the branching program machine is that the function can be stored in a smaller memory than the straightforward single-memory implementation.

Compared with general purpose micro processors, branching program machines are simpler and faster. With H. Nakahara, Sasao developed various machines including ones based on MDDs using FPGAs [92], [94], [95], [99], [109], [114], [119].

F. Numerical Function Generator

Sasao invented LUT cascades, as an efficient realization of a logic function. Since the purpose of the CLUSTER grant was to find practical applications, he focused on numberic function generators. Among them, Sasao invented a systematic method to design numerical function generator using LUT cascades. With S. Nagayama and Jon T. Butler, Sasao developed various function generators [14], [28], [36], [44], [51], [55], [52], [56], [64], [68], [71], [74], [75], [77], [79], [87], [90], [91], [96], [89], [106], [110].

G. Classification Function

Classification functions are used in the internet. It can be implemented by a content addressable memory (CAM). To estimate the size of the CAM, Sasao analyzed the complexity of classification functions [70], [93], [118].

H. Code Converters

As an application of memory-based logic circuits, Sasao considered various code converters. As for radix converters Sasao worked with Y. Iguchi [20], [45], [57], [66], [61], [66]. As for constant-weight code to index converters [113] and index to constant-weight code converters [105], Sasao worked with J. T. Butler. Also, modulo circuits [107], and index to permutation converters [125] were designed.

I. FPGA Design

Field programmable gate arrays (FPGAs) are devices that can be programmed by the user to implement a logic function. Because of their short turnaround time and low development cost, they are extensively used in the products with low volume production. Sasao analyzed the number of LUTs to implement a given type of logic functions [83].

J. Complexity Measures for Logic Functions

Sasao made some contributions to the understanding of the complexity of logic functions. **C-measure** estimates the complexity of LUT-cascade realization [23], [42]. **Average path length** (APL) estimates the time to evaluate the decision diagrams by branching program machines [26], [27].

K. Functional Decomposition

Functional decomposition is an essential technique to design logic circuits, especially in FPGAs. Sasao developed an efficient method to find simple disjoint decompositions by using BDDs. This method has become a standard technique to find functional decomposition: [2], [15], [24]. Recently, he developed a concept of a **linear decomposition** [111], [115], [117], and a **row-shift decomposition** [120]. They are useful for index generation functions.

L. Reconfigurable Logic

Sasao invented various type of reconfigurable logic circuits and their design methods: [58], [60], [69].

M. Spectral Analysis of Logic Functions

With J. T. Butler, Sasao analyzed Reed-Muller transforms that have **igenvalues** [59]. Hardware for Walsh transformation are also considered [12], [21], [33]. Test generation using spectrum is considered in [5].

N. Boolean Matching

Boolean matching is useful in technology mapping in LSI design. D. Debnath and Sasao developed fast Boolean matching algorithms [3], [16], [50], [54]

O. Miscellaneous Projects

In addition to the other projects, Sasao performed miscellaneous projects with other researchers: PLA design [25]; Optimization of AND-EXOR logical expressions [34]; Logic functions for cryptography [81]; Error detection circuit [73]; Circuits for cryptography [18], [39]; Function evaluation [7]; and Robot [22].

II. Research Grants

During the period between FY2004 to FY2012, Sasao obtained the following grants:

CLUSTER (MEXT)

- "Memory-based programmable logic elements and their applications". (April 2002 to March 2007).
- "Realization of high-speed pattern matching circuits and their applications". (Sept. 2007 to March 2012).

KAKEN (JSPS)

- "Logic synthesis using linear transformation and memory". (April 2011 to March 2013).
- "Realization of content addressable memory functions using conventional memory, and their applications". (April 2007 to March 2009).
- "Logic synthesis of look-up table ring". (April 2004 to March 2005).
- "Programmable logic elements using virtual interconnections and their logic synthesis". (April 2002 to March 2004).

Other Donations from industries.

III. Books

During this period, Sasao published two books: one surveys the cascade realization of logic functions and index generation functions [103]. Other is an edited book related to the Reed-Muller Workshop organized by Sasao and Butler in 2009 [88].

IV. People

Many people involved in the project: M. Matsuura (technical stuff); J. T. Butler (visiting researcher); H. Nakahara (Phd student, then research stuff); S. Nagayama (Phd student, then research stuff); Y. Iguchi (visiting researcher); B. Falkowski (visiting researcher); M. Perkowski (visiting researcher); M. Reidel (visiting researcher); A. Mishchenko (visiting researcher); H. Qin (Phd student); K. Nakamura (Professor of KIT); D. Debnath (former Phd. student); A. Iseno (Phd student, then research stuff); I. Syafalni(Phd student) .

V. Awards

Sasao's group received many domestic and international awards. Major awards include:

1) IPSJ Transactions on System LSI Design Methodology Outstanding Paper Award:
   S. Nagayama, T. Sasao, and Jon. T. Butler, "Programmable architectures and design method for two-variable numeric function generators," *IPSJ Transactions on Systems LSI Design Methodology*, Vol. 3, pp.118-129, Feb. 2010.
2) Outstanding Paper Award:
   H. Nakahara, T. Sasao, and M. Matsuura, "A regular expression matching circuit based on a modular non-deterministic finite automaton with multi-character transition," *The 16th Workshop on Synthesis And System Integration of Mixed Information technologies* (SASIMI2010), Taipei, Oct. 18-19, 2010.

3) First Place: Memocode co-design contest:
H. Nakahara, T. Sasao, and M. Matsuura, "A regular expression matching circuit using memories and shift registers," *8th ACM/IEEE International Conference on Formal Methods and Models for Codesign* (MEMOCODE-2010), Grenoble, France, July 26-28, 2010.
4) IEEE Computer Society Japan Chapter Young Author Award 2009 (S. Nagayama):
S. Nagayama and T. Sasao, "Complexities of graph-based representations for elementary functions" *IEEE Transactions on Computers*, Vol. C-58. No.1, pp.106-119, Jan. 2009
5) Outstanding Contributed Paper Award:
S. Nagayama and T. Sasao, "On the minimization of average path lengths for heterogeneous MDDs," *34th International Symposium on Multiple-Valued Logic* (ISMVL-2004), Toronto, Canada, May 19-22, 2004, pp. 216-222.
6) Distinctive Contributed Paper Award:
T. Sasao," Cascade realization of two-valued input three-valued functions using decomposition of group functions," *33rd International Symposium on Multiple-Valued Logic*, Tokyo, May 16-19, 2003, pp.125-132.

REFERENCES

[1] T. Sasao,"Survey of research projects conducted by Sasao's group," Jan. 26, 2004.

[2] T. Sasao and J. T. Butler, "A fast method to derive minimum SOPs for decomposable functions," *Asia and South Pacific Design Automation Conference 2004* (ASP-DAC 2004), Yokohama, Jan. 27-30, 2004, pp. 585-590.

[3] D. Debnath and T. Sasao, " Efficient computation of canonical form for Boolean matching in large libraries," *Asia and South Pacific Design Automation Conference 2004* (ASP-DAC 2004), Yokohama, Jan. 27-30, 2004, pp. 591-596.

[4] S. Nagayama and T. Sasao, "Minimization of memory size for heterogeneous MDDs," *Asia and South Pacific Design Automation Conference 2004* (ASP-DAC 2004), Yokohama, Jan. 27-30, 2004, pp. 872-875.

[5] A. Iseno, Y. Iguchi, and T. Sasao, "Fault diagnosis for RAMs using Walsh spectrum," *IEICE Trans. Information and Systems*, Vol. E87-D, No.3, March 2004, pp. 592-600.

[6] S. Nagayama and T. Sasao, "On the minimization of average path lengths for heterogeneous MDDs," *34th International Symposium on Multiple-Valued Logic* (ISMVL-2004), Toronto, Canada, May 19-22, 2004, pp. 216-222.

[7] Y. Iguchi, T. Sasao, and M. Matsuura, "A method to evaluate logic functions in the presence of unknown inputs using LUT cascades," *34th International Symposium on Multiple-Valued Logic* (ISMVL-2004), Toronto, Canada, May 19-22, 2004, pp. 302-308.

[8] S. Nagayama, T. Sasao, Y. Iguchi, and M. Matsuura, "Area-time complexities of multi-valued decision diagrams," *IEICE Transactions on Fundamentals of Electronics*, Vol.E87-A, No.5, pp. 1020-1028, May, 2004.

[9] T. Sasao, M. Kusano, and M. Matsuura, "Optimization methods in look-up table rings," *International Workshop on Logic and Synthesis* (IWLS-2004), June 2-4, Temecula, California, U.S.A. .pp. 431-437.

[10] S. Nagayama and T. Sasao, "On the minimization of longest path length for decision diagrams," *International Workshop on Logic and Synthesis* (IWLS-2004), June 2-4, Temecula, California, U.S.A., pp. 28-35.

[11] T. Sasao, H. Nakahara, M. Matsuura and Y. Iguchi, "Realization of sequential circuits by look-up table ring," *The 2004 IEEE International Midwest Symposium on Circuits and Systems* (MWSCAS 2004), Hiroshima, July 25-28, 2004, pp.I:517-I:520.

[12] B. Falkowski and T. Sasao, "Implementation of Walsh function generator of order 64 using lut cascades," *The 2004 IEEE International Midwest Symposium on Circuits and Systems* (MWSCAS 2004), Hiroshima, July 25-28, 2004, pp.III:447-III:450.

[13] H. Nakahara, T. Sasao, and M. Matsuura, "A design algorithm for sequential circuits using LUT rings," *The 12th Workshop on Synthesis And System Integration of Mixed Information technologies* (SASIMI2004), Oct. 18-19, 2004, Kanazawa, Japan, pp.430-437.

[14] T. Sasao, J. T. Butler, and M. D. Riedel, "Application of LUT cascades to numerical function generators," *The 12th Workshop on Synthesis And System Integration of Mixed Information technologies* (SASIMI2004), Oct. 18-19, 2004, Kanazawa, Japan, pp.422-429.

[15] T. Sasao and M. Matsuura, "A method to decompose multiple-output logic functions," *41st Design Automation Conference*, San Diego, CA, USA, June 2-6, 2004, pp.428-433.

[16] D. Debnath and T. Sasao, "Fast Boolean matching under permutation by efficient computation of canonical form," *IEICE Transactions on Fundamentals of Electronics*, Vol.E87-A, Dec. 2004, pp.3134-3140.

[17] H. Qin, T. Sasao, M. Matsuura, K. Nakamura, S. Nagayama and Y. Iguchi, "A realization of multiple-output functions by a look-up table ring," *IEICE Transactions on Fundamentals of Electronics*, Vol.E87-A, Dec. 2004, pp.3141-3150.

[18] H. Qin, T. Sasao, and Y. Iguchi, "An FPGA design of AES encryption circuit with 128-bit keys," *GLSVLSI 2005*, Chicago, IL, April 17-19, 2005, pp. 147-151.

[19] K. Nakamura, T. Sasao, M. Matsuura, K. Tanaka, K. Yoshizumi, H. Qin, and Y. Iguchi, "Programmable logic device with an 8-stage cascade of 64K-bit asynchronous SRAMs," *IEEE Symposium on Low-Power and High-Speed Chips* (Cool Chips VIII), April 20-22, 2005, Yokohama, Japan. Slides

[20] T. Sasao,"Radix converters: Complexity and implementation by LUT cascades," *ISMVL-2005*, May 19-21, 2005, Calgary, Canada, pp.256-263.

[21] Y. Iguchi and T. Sasao, "Hardware to compute Walsh coefficients," *ISMVL-2005*, May 19-21, 2005, Calgary, Canada, pp.75-81.

[22] M. Perkowski, T. Sasao, J-H. Kim, M. Lukac, J. Allen, and S. Gebauer, "Hahoe KAIST robot theater: Learning rules of interactive robot behavior as a multi-valued logic synthesis problem," *ISMVL-2005*, May 19-21, 2005, Calgary, Canada, pp.236-248.

[23] T. Sasao, "Analysis and synthesis of weighted-sum functions," *International Workshop on Logic and Synthesis* (IWLS-2005), Lake Arrowhead, CA, USA, June 8-10, 2005,pp.455-462.

[24] T. Sasao and M. Matsuura, "BDD representation for incompletely specified multiple-output logic functions and its applications to functional decomposition," *Design Automation Conference*, June 2005, pp.373-378.

[25] D. Debnath and T. Sasao, "Output phase optimization for AND-OR-EXOR PLAs with decoders and its application to design of adders,"*IEICE Transactions on Information and Systems*, Vol. E88-D. No. 7, July 2005, pp.1492-1500.

[26] S. Nagayama, A. Mishchenko, T. Sasao, and J. T. Butler, "Exact and heuristic minimization of the average path length in decision diagrams," *Journal of Multiple-Valued Logic and Soft Computing*, Vol.11, No.5-6, pp.437-465, Aug. 2005. 1 2

[27] J. T. Butler, T. Sasao, and M. Matsuura, "Average path length of binary decision diagrams," *IEEE Transactions on Computers*, Vol. 54, No.9, pp.1041-1053, Sept. 2005.

[28] T. Sasao, S. Nagayama, and J. T. Butler, "Programmable numerical function generators: Architectures and synthesis system," *FPL2005*, Tampere, Aug.24-26, 2005, pp.118-123.

[29] T. Sasao, Y. Iguchi, T. Suzuki, "On LUT cascade realizations of FIR filters," *8th Euromicro Conference on Digital System Design: Architectures, Methods and Tools* (DSD2005), Porto, Portugal, Aug. 30 - Sept. 3, 2005, pp.467-474.

[30] K. Nakamura, T. Sasao, M. Matsuura, K. Tanaka, K. Yoshizumi, H. Nakahara, and Y. Iguchi, "A memory-based programmable logic device using a look-up table cascade with synchronous SRAMs," *2005 International Conference on Solid State Devices and Materials* (SSDM 2005), Kobe, Japan, Sep. 2005.

[31] T. Sasao, Y. Iguchi, M. Matsuura, "LUT cascades and emulators for realizations of logic functions," *RM2005*, Tokyo, Japan, Sept. 5 - Sept. 6, 2005, pp.63-70.

[32] S. Nagayama, and T. Sasao, "On the optimization of heterogeneous

MDDs," IEEE Transactions on CAD, Vol. 24, No.11, Nov. 2005, pp.1645-1659.

[33] B. Falkowski and T. Sasao, "Unified algorithm to generate Walsh functions in four different orderings and its programmable hardware implementation," *IEE Proc. Vision, Image & Signal Processing*, Vol. 152, No.6, Dec. 2005, pp.819-826.

[34] D. Debnath and T. Sasao, "Exact minimization of FPRMs for incompletely specified functions by using MTBDDs," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, Vol. E88-A, No.12, Dec. 2005, pp.3332-3341.

[35] H. Nakahara, T. Sasao, and M. Matsuura, "A design algorithm for sequential circuits using LUT rings," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, Vol. E88-A, No.12, Dec. 2005, pp.3342-3350.

[36] S. Nagayama, T. Sasao, and J. T. Butler, "Programmable numerical function generators based on quadratic approximation: Architecture and synthesis method," *ASPDAC 2006*, Yokohama Jan. 2006, pp. 378-383.

[37] H. Nakahara, T. Sasao and M. Matsuura, "A fast logic simulator using an LUT cascade emulator," *ASPDAC 2006*, Yokohama Jan. 2006, pp.466-465.

[38] H. Qin, T. Sasao, and J. T. Butler, "Implementation of LPM address generator on FPGAs," *International Workshop on Applied Reconfigurable Computing* (ARC2006) Delft, the Netherlands, March 1-3, 2006. Also appeared in Lecture Notes in Computer Science 3985, pp.170-181.

[39] H. Qin, T. Sasao and Y. Iguchi, "A design of AES encryption circuit with 128-bit keys using look-up table ring on FPGA," *IEICE Trans. on Information and Systems*, Vol.E89-D, No.3, March 2006, pp.1139-1147.

[40] H. Qin and T. Sasao, "Design of address generators using multiple LUT cascade on FPGA," *SASIMI Workshop*, April 2006, Nagoya, Japan, pp.146-152.

[41] K. Nakamura, T. Sasao, M. Matsuura, K. Tanaka, K. Yoshizumi, H. Nakahara and Y. Iguchi, "A memory-based programmable logic device using look-up table cascade with synchronous static random access memories," *Japanese Journal of Applied Physics*, Vol. 45, No. 4B, 2006, pp. 3295-3300. April, 2006.

[42] T. Sasao, "Analysis and synthesis of weighted-sum functions," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 5, May 2006, pp. 789 - 796.

[43] T. Sasao and J. T. Butler, "Implementation of multiple-valued CAM functions by LUT cascades," *ISMVL-2006*, Singapore, May 17-20, 2006.

[44] T. Sasao and S. Nagayama, "Representations of elementary functions using binary moment diagrams," *ISMVL-2006*, Singapore, May 17-20, 2006.

[45] Y. Iguchi, T. Sasao, and M. Matsuura, "On designs of radix converters using arithmetic decompositions," *ISMVL-2006*, Singapore, May 17-20, 2006.

[46] T. Sasao, "Design methods for multiple-valued input address generators," *ISMVL-2006* (invited paper), Singapore, May 17-20, 2006.

[47] T. Sasao, "A Design method of address generators using hash memories," *IWLS-2006*, Vail, Colorado, U.S.A, June 7-9, 2006, pp.102-109.

[48] H. Nakahara and T. Sasao, "A soft error tolerant LUT cascade emulator," *The Fifteenth Asian Test Symposium*, (ATS-2006), Nov. 20-23, 2006, pp.115-121, Fukuoka, JAPAN.

[49] H. Nakahara and T. Sasao, "A PC-based logic simulator using a look-up table cascade emulator," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, Vol. E89-A, No.12, Dec. 2006, pp.3471-3481.

[50] D. Debnath and T. Sasao, "Efficient computation of canonical form under variable permutation and negation for Boolean matching in large libraries," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, Vol. E89-A, No.12, Dec. 2006, pp.3443-3450.

[51] S. Nagayama, T. Sasao, and J. T. Butler,"Compact numerical function generators based on quadratic approximation: architecture and synthesis method," *IEICE Transactions on Fundamentals of Electronics, Communications and Computer Sciences*, Vol. E89-A, No.12, Dec. 2006, pp.3510-3518.

[52] S. Nagayama, T. Sasao, and J. T. Butler, "Numerical function generators using edge-valued binary decision diagrams," *ASPDAC-2007*,Yokohama, Jan. 25, 2007, pp.535-540.

[53] H. Nakahara, T. Sasao and M. Matsuura, "A CAM emulator using look-up table cascades," *14th Reconfigurable Architectures Workshop* (RAW 2007), March 2007, Long Beach California, USA. CD-ROM RAW-9-paper-2,

[54] D. Debnath and T. Sasao, "A new equivalence relation of logic functions and its application in the design of AND-OR-EXOR networks," *IEICE Transaction on Fundamentals of Electronics, Communications and Computer Sciences*, Vol.E90-A. No.5, May 2007, pp.932-940.

[55] T. Sasao, S. Nagayama and J. T. Butler, "Numerical function generators using LUT cascades," *IEEE Transactions on Computers*, Vol.56, No.6, June 2007, pp.826-838.

[56] S. Nagayama and T. Sasao, "Representations of elementary functions using edge-valued MDDs," *ISMVL-2007*, Oslo, Norway, May 13-16, 2007.(CD-ROM)

[57] Y. Iguchi, T. Sasao, and M. Matsuura, "On designs of radix converters using arithmetic decompositions," *ISMVL-2007*, Oslo, Norway, May 13-16, 2007.(CD-ROM)

[58] T. Sasao, "An Application of 16-Valued logic to design of reconfigurable logic arrays," *ISMVL-2007*, Oslo, Norway, May 13-16, 2007.(CD-ROM)

[59] T. Sasao and J.T. Butler, "The eigenfunction of the Reed-Muller transformation," *RM-2007*, Oslo, Norway, May 16, 2007.

[60] T. Sasao, "Sum-of-generalized products expressions: Applications and minimization," *IWLS-2007*, San Diego, California, U.S.A, May 30-June 1, 2007, pp.372-379.

[61] Y. Iguchi, T. Sasao, and M. Matsuura, "Design methods of radix converters using arithmetic decompositions," *IEICE Trans. on Information and Systems*, Vol.E90-D, No.6, June 2007, pp.905-914.

[62] H. Qin, T. Sasao, and J. T. Butler, "On the design of LPM address generators using multiple LUT Cascades on FPGAs," *International Journal of Electronics*, Vol. 94, Issue 5, May 2007, pp.451-467,

[63] T. Sasao and M. Matsuura,"An implementation of an address generator using hash memories," *10th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools* (DSD 2007), Aug. 27 - 31, 2007, Lubeck, Germany, pp.69-76.

[64] S. Nagayama, T. Sasao, and J. T. Butler, "Design method of numerical function generators based on polynomial approximation for FPGA implementation," *10th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools*, (DSD 2007) ,Aug. 27 - 31, 2007, Lubeck, Germany, pp. 280-287.

[65] H. Nakahara, T. Sasao, and M. Matsuura, "A hybrid logic simulator using LUT cascade emulators," *The 14th Workshop on Synthesis And System Integration of Mixed Information technologies* (SASIMI 2007), Sapporo, Japan, Oct 15-16, 2007, pp.135-141.

[66] Y. Iguchi, T. Sasao, and M. Matsuura, "Design methods for binary to decimal converters using arithmetic decompositions," *Journal of Multiple-Valued Logic*, Vol.13, No.4-6, 2007, pp.503-520.

[67] M. Matsuura and T. Sasao, "BDD representation for incompletely specified multiple-output logic functions and its application to the design of LUT cascades," *IEICE Transaction on Fundamentals of Electronics, Communications and Computer Sciences*, Vol.E90-A, No.12, Dec. 2007, pp.2770-2777.

[68] S. Nagayama, T. Sasao, and J. T. Butler, "Design method for numerical function generators using recursive segmentation and EVBDDs," *IEICE Transaction on Fundamentals of Electronics, Communications and Computer Sciences*, Vol.E90-A, No.12, Dec. 2007, pp.2752-2761.

[69] T. Sasao and H. Nakahara, "Implementations of reconfigurable logic arrays on FPGAs," *International Conference on Field-Programmable Technology 2007* (ICFPT'07) , Dec. 12-14, 2007, Kitakyushu, Japan, pp.217-223.

[70] T. Sasao, "On the complexity of classification functions," *International Symposium on Multiple-valued Logic* (ISMVL-2008), Dallas, TX, May 22-24, 2008 CD-ROM

[71] S. Nagayama, and T. Sasao, "Representations of two-variable elementary functions using EVMDDs and their applications to function generators," *International Symposium on Multiple-valued Logic* (ISMVL-2008), Dallas, TX, May 22-24, 2008 CD-ROM

[72] T. Sasao, "On the number of variables to represent sparse logic functions," *17th International Workshop on Logic & Synthesis* (IWLS-2008), Lake Tahoe, California, USA, June 4-6, 2008, pp.233-239.

[73] T. Sasao and Y. Iguchi, "On the complexity of single-digit error detection function in redundant residue number system, "*10th EUROMICRO Conference on Digital System Design, Architectures,*

Methods and Tools (DSD-2008), Sept. 1 - 5, 2008, Parma, Italy. pp.880-887.

[74] S. Nagayama, J. T. Butler, and T. Sasao, "Programmable numerical function generators for two-variable functions," *10th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools* (DSD 2008), Sept. 1 - 5, 2008, Parma, Italy, pp.891-898.

[75] S. Nagayama, T. Sasao, and J. T. Butler, "Numerical function generators using bilinear interpolation," *FPL-2008*, Heidelberg, Germany, Sept. 8-10, 2008, pp.463-466.

[76] T. Sasao, "On the number of variables to represent sparse logic functions," *ICCAD-2008*, San Jose, California, USA, Nov.10-13, 2008, pp. 45-51.

[77] S. Nagayama and T. Sasao, "Complexities of graph-based representations for elementary functions," *IEEE Transactions on Computers*, Vol. C-58. No. 1, Jan. 2009, pp.106-119.

[78] H. Nakahara, T. Sasao, M. Matsuura, and Y. Kawamura, "Emulation of sequential circuits by a parallel branching program machine," *5th International Workshop on Applied Reconfigurable Computing*, Karlsruhe, Germany, March 16-18, 2009. Lecture Notes in Computer Science, LNCS5443, pp. 261-267, March 2009.

[79] S. Nagayama, and T. Sasao, and J. T. Butler, "Floating-point numerical function generators using EVMDDs for monotone elementary functions," *39th International Symposium on Multiple-Valued Logic* (ISMVL 2009) May 21-23, 2009, pp.349-355.

[80] T. Sasao, H. Nakahara, M. Matsuura, Y. Kawamura, and J. T. Butler, "A quaternary decision diagram machine and the optimization of its code," *39th International Symposium on Multiple-Valued Logic* (ISMVL 2009), May 21-23, 2009,pp.362-369.

[81] J. T. Butler and T. Sasao, "Logic functions for cryptography - A tutorial," *Reed-Muller Workshop* (RM2009), pp.127-136, May 23-24, 2009.

[82] T. Sasao,"On the number of LUTS to realize sparse logic functions," *18th International Workshop on Logic and Synthesis*, (IWLS-2009), Berkeley, CA, U.S.A., July 31-Aug. 2, 2009, pp.64-71.

[83] T. Sasao and A. Mishchenko,"LUTMIN: FPGA logic synthesis with MUX-based and cascade realizations," *18th International Workshop on Logic and Synthesis*, (IWLS-2009), Berkeley, CA, U.S.A., July 31-Aug. 2, 2009, pp.310-316

[84] H. Nakahara, T. Sasao, , M. Matsuura, and Y. Kawamura, "The Parallel sieve method for a virus scanning engine," *12th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools*(DSD 2009) , Patras, Greece , Aug. 27-29, 2009, pp.809-816.

[85] T. Sasao, T. Nakamura, and M. Matsuura, "Representation of incompletely specified index generation functions using minimal number of compound variables," *12th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools* (DSD 2009), Patras, Greece, Aug. 27-29, 2009, pp.765-772.

[86] H. Nakahara, T. Sasao, M. Matsuura, and Y. Kawamura, "A virus scanning engine using a parallel finite-input memory machines and MPUs," *19th International Conference on Field Programmable Logic and Applications*, (FPL-2009), Prague. Czech Republic, Aug. 31-Sept. 2, 2009.

[87] S. Nagayama, T. Sasao, and J. T. Butler, "Numerical function generators using decision diagrams for discrete functions," *Proceedings of the 18th International Workshop on Post-Binary ULSI Systems*, May 20, 2009, Naha, Okinawa, Japan.

[88] T. Sasao and J. T. Butler, (ed) *Progress in Applications of Boolean Functions,* Morgan & Claypool Publishers, Jan 2010. pp.1-153. (Digital Circuits & Systems Series)

[89] C. L. Frenzen, T. Sasao, and J. T. Butler, "On the number of segments needed in a piecewise linear approximation," *Jour. of Computational and Applied Mathematics*, Volume 234, Issue 2, 15 May 2010, pp. 437-446.

[90] S. Nagayama, T. Sasao and J. T. Butler, "Programmable Architectures and design methods for two-variable numeric function generators," *IPSJ Transactions on System LSI Design Methodology*, Vol. 3, pp.118-129, Feb. 2010.

[91] S. Nagayama, T. Sasao and J. T. Butler, "Floating-point numeric function generators based on piecewise-split EVMDDs," *International Symposium on Multiple-Valued Logic*, Barcelona, Spain, May 26-28, 2010, pp.223-228.

[92] H. Nakahara, T. Sasao and M. Matsuura, "A comparison of architectures for various decision diagram machines,"*International Symposium on Multiple-Valued Logic*, Barcelona, Spain, May 26-28, 2010, pp.229-234.

[93] T. Sasao, "On the number of products to represent interval functions by SOPs with four-valued variables," *International Symposium on Multiple-Valued Logic*, Barcelona, Spain, May 26-28, 2010, pp.282-287.

[94] T. Sasao, H. Nakahara, M. Matsuura, Y. Kawamura, and J. T. Butler, "A quaternary decision diagram machine: Optimization of its code," *IEICE Transactions on Information and Systems*, Vol. E93-D No. 8 pp. 2026-2035, Aug. 2010.

[95] H. Nakahara, T. Sasao, M. Matsuura, and Y. Kawamura, "A parallel branching program machine for sequential circuits: Implementation and evaluation," *IEICE Transactions on Information and Systems*, Vol. E93-D No. 8 pp. 2048-2058, Aug. 2010.

[96] S. Nagayama, T. Sasao and J. T. Butler, "Systematic design method for two-variable numeric function generators using multiple-valued decision diagrams," *IEICE Transactions on Information and Systems*, Vol. E93-D No. 8 pp. 2059-2067, Aug. 2010.

[97] T. Sasao, M. Matsuura and H. Nakahara, "A realization of index generation functions using modules of uniform sizes," *19th International Workshop on Logic and Synthesis* (IWLS-2010), June 18-20, 2010, pp.201-208.

[98] H. Nakahara, T. Sasao, and M. Matsuura, "A regular expression matching using non-deterministic finite automaton," *Proc. of Eighth ACM/IEEE International Conference on Formal Methods and Models for Codesign*, (MEMOCODE-2010) Grenoble, France, July 26-28, 2010, pp.73-76.

[99] H. Nakahara, T. Sasao, and M. Matsuura, "Packet classifier using a parallel branching program machine," *13th EUROMICRO Conference on Digital System Design* (DSD-2010) Lille, France, Sept. 1-3, 2010, pp.745-752.

[100] T. Sasao, "On the numbers of variables to represent multi-valued incompletely specified functions," *13th EUROMICRO Conference on Digital System Design* (DSD-2010) Lille, France, Sept. 1-3, 2010, pp.420-423.

[101] H. Nakahara, T. Sasao, and M. Matsuura,"A regular expression matching circuit based on a modular non-deterministic finite automaton with multi-character transition," *The 16th Workshop on Synthesis And System Integration of Mixed Information technologies* (SASIMI-2010), Taipei, Oct. 18-19, 2010, pp. 359 - 364.

[102] T. Sasao, "Index generation functions: theory and applications," *2010 International Symposium on Communications and Information Technologies*, (ISCIT-2010), Tokyo, Oct. 26-29. 2010, THA1-3-1, pp.585-590.

[103] T. Sasao, *Memory-Based Logic Synthesis*, Springer, March 2011.

[104] H. Nakahara, T. Sasao and M. Matsuura, "A regular expression matching circuit based on a decomposed automaton,"*7th International Symposium on Applied Reconfigurable Computing*, (ARC 2011), March 23-25, 2011, Belfast. Lecture Notes in Computer Science , 6578, pp.16-28.

[105] J. T. Butler and T. Sasao, "Index to constant weight codeword converter,"*7th International Symposium on Applied Reconfigurable Computing*, (ARC 2011), March 23-25, 2011, Belfast. Lecture Notes in Computer Science , 6578, pp.193-205.

[106] J. T. Butler, C.L.Frenzen, N.Macaria, and T. Sasao, "A fast segmentation algorithm for piecewise polynomial numeric function generators,"*Journal of Computational and Applied Mathematics*, Vol. 235, Issue14, pp.4076-4082, May 2011.

[107] J. T. Butler and T. Sasao, "Fast hardware computation of x mod z,"*18th Reconfigurable Architectures Workshop* (RAW 2011), May 16-17, 2011, Anchorage, Alaska, USA.

[108] T. Sasao, "Index generation functions: Theory and application"(invited paper), *International Symposium on Multiple-Valued Logic* (ISMVL-2011), Tuusula, Finland, May 23-25, 2011.

[109] H. Nakahara, T. Sasao and M. Matsuura, "A Comparison of heterogeneous multi-valued decision diagram machines for multiple-output logic functions,"*International Symposium on Multiple-Valued Logic* (ISMVL-2011), Tuusula, Finland, May 23-25, 2011.

[110] S. Nagayama, T. Sasao, and J. T. Butler, "Numeric function generators using piecewise arithmetic expressions,"*International Symposium on Multiple-Valued Logic* (ISMVL-2011), Tuusula, Finland, May 23-25, 2011.

[111] T. Sasao, "Linear transformations for variable reduction," *Reed-Muller 2011 Workshop*, Tuusula, Finland, May 25-26, 2011.

[112] T. Sasao, "Linear decomposition of logic functions: Theory and applications,"*The 20th International Workshop on Logic and Synthesis*, San Diego, June 3 - 5, 2011.

[113] J. T. Butler and T. Sasao, "Fast constant weight codeword to index converter,"*The 54th IEEE International Midwest Symposium on Circuits and Systems* (MWCAS-2011), Korea August 7-10, 2011.

[114] H. Nakahara, T. Sasao, and M. Matsuura, "On a prefetching heterogeneous MDD machine,"" *The 54th IEEE International Midwest Symposium on Circuits and Systems* (MWSCAS-2011), Korea August 7-10, 2011.

[115] T. Sasao, "Linear decomposition of index generation functions," *17th Asia and South Pacific Design Automation Conference* (ASPDAC-2012), Jan. 30- Feb. 2, 2012, Sydney, Australia, pp.781-788.

[116] H. Nakahara, T. Sasao, and M. Matsuura, "A design method of a regular expression matching circuit based on decomposed automaton," *IEICE Transactions on Information and Systems*, Vol. E95-D, No.2, pp.364-373.

[117] T. Sasao, M. Maeta, R. S. Stankovic, and S. Stankovic, "Affine transformations of logic functions and their application to affine decompositions of index generation functions," *The 17th Workshop on Synthesis And System Integration of Mixed Information technologies* (SASIMI-2012), March 8-9, 2012, Beppu, Ohita, Japan.

[118] I. Syfalni and T. Sasao,"Head-tail expressions for interval functions," *The 17th Workshop on Synthesis And System Integration of Mixed Information technologies* (SASIMI-2012), March 8-9, 2012, Beppu, Ohita, Japan.

[119] H. Nakahara, T. Sasao, and M. Matsuura, "A low power-delay product processor using multiple-valued decision diagram machine," *The 17th Workshop on Synthesis And System Integration of Mixed Information technologies* (SASIMI-2012), March 8-9, 2012, Beppu, Ohita, Japan.

[120] T. Sasao, "Row-shift decompositions for index generation functions," *Design, Automation & Test in Europe* (DATE-2012), March 12-16, 2012, Dresden, Germany.

[121] H. Nakahara, T. Sasao, and M. Matsuura, "A low-cost and high-performance virus scanning engine using a binary CAM emulator and an MPU," *8th International Symposium on Applied Reconfigurable Computing*, (ARC 2012), March 19-23, 2012, Hong-Kong. Also, *Lecture Notes in Compute Science*, Vol. xxxxxxx.

[122] T. Sasao, "Multiple-valued input index generation functions: Optimization by linear transformation," *International Symposium on Multiple-Valued Logic* (ISMVL-2012), Victoria, Canada, May 14-16, 2012.

[123] S. Nagayama, T. Sasao, and J. T. Butler,"Analysis of multi-state systems with multi-state components using EVMDDs," *International Symposium on Multiple-Valued Logic* (ISMVL-2012), Victoria, Canada, May 14-16, 2012.

[124] H. Nakahara, T. Sasao, and M. Matsuura, "Multi-terminal multiple-valued decision diagrams for characteristic function representing cluster decomposition," *International Symposium on Multiple-Valued Logic* (ISMVL-2012), Victoria, Canada, May 14-16, 2012.

[125] J. T. Butler and T. Sasao, "Hardware Index to Permutation Converter," *19th Reconfigurable Architectures Workshop*, May 21-22, 2012, Shanghai, China.