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Abstract—This paper surveys research projects conducted by Prof. Tsutomu Sasao’s group during FY2004 to FY2011. The research projects in this period can be divided into the following groups: 1) Cascade realizations; 2) Index generation functions; 3) Pattern matching circuits; 4) Decision diagrams; 5) Branching program machines; 6) Numerical function generators; 7) Classification functions; 8) Code converters; 9) FPGA designs; 10) Complexity measures for logic functions; 11) Functional decompositions; 12) Reconfigurable logic; 13) Spectral analysis of logic functions; 14) Boolean matching; and 15) Miscellaneous Projects.

I. Projects

A. Cascade Realization

Like the programmable logic array (PLA), a cascade has a regular structure, and is easier to design than random logic networks. Sasao found an efficient method to map a logic function represented by a binary decision diagram (BDD) into a cascade of lookup tables (or LUT cascade). He also invented a method to realize multiple-output logic function using a large (LUT) and a sequencer [9], [11], [13], [17], [19], [30], [31], [29], [35], [37], [48], [49], [41], [53], [65], [67], [82].

B. Index Generation Function

The most difficult task of the project was to find killer applications of LUT cascades. For this purpose, Sasao worked with Yamaha Corporation. An engineer of Yamaha suggested to apply it as an address generator in computer networks. This was the seminal idea in the project. From this, Sasao formulated the concept of index generation functions [38], [40], [43], [46], [47], [62], [63], [72], [76], [80], [84], [85], [97], [100], [102], [103], [108], [111], [112]. Afterwards, a cooperative project with Renesas Electronics Corporation was conducted.

C. Pattern Matching Circuits

In the second stage of the CLUSTER project (FY2007-FY2012), Sasao developed fast pattern matching circuits. It is a good application of LUT cascades developed in the first stage (FY2002 to FY2007). With H. Nakahara, Sasao developed exact matching and regular expression matching circuits [53], [78], [80], [86], [98], [101], [104], [116], [121]. Major applications of index generation function include: address tables in the internet, terminal access controllers, memory patches, code converters, scanning engines for computer virus, DNA matching, and text compressions.

D. Decision Diagrams

One of the most important problems in logic synthesis is to represent logic functions compactly while maintaining low delay. Binary decision diagrams (BDDs) are such representations. With S. Nagayama, Sasao considered various decision diagrams to represent logic functions: Multi-valued decision diagrams (MDDs), and heterogeneous MDD [10], [6], [4], [8].

E. Branching Program Machines

Branching program machines are circuits that evaluate logic function represented by decision diagrams. Sasao investigated a circuit that evaluates each type of decision diagram. The advantage of the branching program machine is that the function can be stored in a smaller memory than the straightforward single-memory implementation.

Compared with general purpose micro processors, branching program machines are simpler and faster. With H. Nakahara, Sasao developed various machines including ones based on MDDs using FPGAs [92], [94], [95], [99], [109], [114], [119].

F. Numerical Function Generator

Sasao invented LUT cascades, as an efficient realization of a logic function. Since the purpose of the CLUSTER grant was to find practical applications, he focused on numeric function generators. Among them, Sasao invented a systematic method to design numerical function generator using LUT cascades. With S. Nagayama and Jon T. Butler, Sasao developed various function generators [14], [28], [36], [44], [51], [55], [52], [56], [64], [68], [71], [74], [75], [77], [79], [87], [90], [91], [96], [89], [106], [110].

G. Classification Function

Classification functions are used in the internet. It can be implemented by a content addressable memory (CAM). To estimate the size of the CAM, Sasao analyzed the complexity of classification functions [70], [93], [118].
H. Code Converters

As an application of memory-based logic circuits, Sasao considered various code converters. As for radix converters Sasao worked with Y. Iguchi [20], [45], [57], [66], [61], [66]. As for constant-weight code to index converters [113] and index to constant-weight code converters [107], Sasao worked with J. T. Butler. Also, modulo circuits [107], and index to permutation converters [125] were designed.

I. FPGA Design

Field programmable gate arrays (FPGAs) are devices that can be programmed by the user to implement a logic function. Because of their short turnaround time and low development cost, they are extensively used in the products with low volume production. Sasao analyzed the number of LUTs to implement a given type of logic functions [83].

J. Complexity Measures for Logic Functions

Sasao made some contributions to the understanding of the complexity of logic functions. C-measure estimates the complexity of LUT-cascade realization [23], [42]. Average path length (APL) estimates the time to evaluate the decision diagrams by branching program machines [26], [27].

K. Functional Decomposition

Functional decomposition is an essential technique to design logic circuits, especially in FPGAs. Sasao developed an efficient method to find simple disjoint decompositions by using BDDs. This method has become a standard technique to find functional decomposition: [2], [15], [24]. Recently, he developed a concept of a linear decomposition [111], [115], [117], and a row-shift decomposition [120]. They are useful for index generation functions.

L. Reconfigurable Logic

Sasao invented various type of reconfigurable logic circuits and their design methods: [58], [60], [69].

M. Spectral Analysis of Logic Functions

With J. T. Butler, Sasao analyzed Reed-Muller transforms that have eigenvalues [59]. Hardware for Walsh transformation are also considered [12], [21], [33]. Test generation using spectrum is considered in [5].

N. Boolean Matching

Boolean matching is useful in technology mapping in LSI design. D. Debnath and Sasao developed fast Boolean matching algorithms [3], [16], [50], [54]

O. Miscellaneous Projects

In addition to the other projects, Sasao performed miscellaneous projects with other researchers: PLA design [25]; Optimization of AND-EXOR logical expressions [34]; Logic functions for cryptography [81]; Error detection circuit [73]; Circuits for cryptography [18], [39]; Function evaluation [7]; and Robot [22].

II. Research Grants

During the period between FY2004 to FY2012, Sasao obtained the following grants:

**CLUSTER (MEXT)**
- "Memory-based programmable logic elements and their applications". (April 2002 to March 2007).
- "Realization of high-speed pattern matching circuits and their applications". (Sept. 2007 to March 2012).

**KAKEN (JSPS)**
- "Logic synthesis using linear transformation and memory". (April 2011 to March 2013).
- "Realization of content addressable memory functions using conventional memory, and their applications". (April 2007 to March 2009).

Other Donations from industries.

III. Books

During this period, Sasao published two books: one surveys the cascade realization of logic functions and index generation functions [103]. Other is an edited book related to the Reed-Muller Workshop organized by Sasao and Butler in 2009 [88].

IV. People

Many people involved in the project: M. Matsuura (technical stuff); J. T. Butler (visiting researcher); H. Nakahara (Phd student, then research stuff); S. Nagayama (Phd student, then research stuff); Y. Iguchi (visiting researcher); B. Falkowski (visiting researcher); M. Perkowski (visiting researcher); M. Reidel (visiting researcher); A. Mishchenko (visiting researcher); H. Qin (Phd student); K. Nakamura (Professor of KIT); D. Debnath (former Phd. student); A. Iseno (Phd student, then research stuff); I. Syafalni(Phd student) .

V. Awards

Sasao’s group received many domestic and international awards. Major awards include:

1) IPSJ Transactions on System LSI Design Methodology Outstanding Paper Award:

2) Outstanding Paper Award:
3) First Place: Memocode co-design contest:

4) IEEE Computer Society Japan Chapter Young Author Award 2009 (S. Nagayama):

5) Outstanding Contributed Paper Award:

6) Distinctive Contributed Paper Award:

REFERENCES


