# Survey of Research Projects Conducted by Sasao's Group.

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## Abstract

This paper surveys research conducted by Prof. Tsutomu Sasao's group on the design of combinational logic circuits. The research projects can be roughly divided into the following groups: 1) Conservative logic circuits; 2) AND-OR two-level logic networks; 3) Logic design using EXOR gates; 4) Representation of logic functions using decision diagrams; 5) Functional decompositions; 6) Cascade realizations; 7) Complexity of logic networks; 8) Design of three-level networks; 9) Easily Testable designs; 10) FPGA designs; 11) Spectral analysis of logic functions; and 12) Others.

## 1 Conservative Logic Circuits

Conservative logic is a model of computation which explicitly reflects a number of fundamental principles of physics, such as the reversibility of the dynamical laws and the conservation of certain additive quantities [137].

Prof. Sasao's series of IEEETC papers [142, 143, 145, 146] (1976-1979) on conservative logic circuits contain a class of reversible computation circuits. His work opened an important research area on theoretical computing defined later by Fredkin and Toffoli [137].

## 2 AND-OR Two-Level Logic Networks

An arbitrary logic function can be realized by an AND-OR two-level circuit. In integrated circuits, two-level circuits are often realized as programmable logic arrays (PLA's). Because PLAs have regular structure, they are easy to design, easy to modify, and easy to test.

In [138], Sasao showed the use of decoders on the input of PLA's. This insight allowed PLA's to be made with 20%-25% fewer components. In [134], he formulated the optimization problem for these improved PLA's. That is, he showed a way to choose variables for the decoders to produce near-minimal PLA's. With these heuristic approaches, he demonstrated that PLA size can be reduced by 30% over PLA's without decoders. In the same paper, he also formulated "the output phase optimization problem of PLA's," and proposed a heuristic method to obtain near-optimum solutions. The output phase optimization technique often reduces the size of PLA's considerably. This method was used to design PLA's of commercial microprocessors including INTEL 80386 [127]. He also presented a fast algorithm to detect all the essential prime implicants. Fast essential prime implicant detection is quite important in logic minimization programs. ESPRESSO [157], a widely used logic minimization program, uses SASAO's method.

In [131], Sasao developed an algorithm to find an AND-OR expression of the complement of a given AND-OR expression. This algorithm is essential to the minimization of large PLA's. He developed an algorithm that is 10 to 20 times faster than a conventional technique. This algorithm has made it possible to minimize large PLA's that could not minimized by previous algorithms because of large computation times and excessive memory requirements.

His books [52, 88] comprehensively describe these PLA design methods. He has applied his methods to multiple-valued PLA's [118, 122], and has applied minimization of multiple-valued functions to binary PLA's [125].

He also developed a logic minimization method using tautology checking [132, 133].

## 3 Logic Design using EXOR gates

Most logic synthesis tools use AND and OR gates as basic logic elements. Arithmetic and error correcting circuits can be realized with many fewer gates, if EXOR gates are available as well as AND and OR gates. Such circuits can be derived from AND-EXOR two-level circuits. So the minimization of Exclusive-OR sum-of-products expressions (ESOPs), which corresponds to the minimization of AND-EXOR two-level circuits, is important.

During 1990-1992, Sasao developed a heuristic minimization algorithm for AND-EXOR logic circuits called EXMIN2

[105], and demonstrated that AND-EXOR circuits require fewer gates than AND-OR circuits to realize arithmetic functions. These results are included in the three IEEE Transaction papers [120, 105, 106], as well as his book [116] published in 1993.

He also invented an elegant method to design AND-OR-EXOR circuits. For arithmetic circuits, his method produces about 50% smaller circuits than conventional AND-OR method [123].

He also obatained exact minimum AND-EXOR expressions with N. Koda [76, 93, 109, 112].

# 4 Representation of Logic Functions by using Decision Diagrams

One of the most important problems in logic synthesis is to represent logic functions compactly, while keeping the speed of manipulation. Binary decision diagrams (BDDs) are such representations.

Sasao considered various decision diagrams to represent logic functions: Decision diagrams using EXOR operators [91], and ternary decision diagrams (TDDs) [65], and multi-valued decision diagrams (MDDs) [41]. He organized a symposium on decision diagrams and published a book [79]. He also considered various methods to represent multiple-output functions [24, 25, 39, 44, 51, 60].

With S. Nagayama, he invented heterogeneous MDD [15, 4, 10].

# 5 Functional Decomposition

Functional decomposition is also essential to design logic circuits, especially in FPGAs. Sasao developed an efficient method to find simple disjoint decompositions by using BDDs [113]. This method has become a standard technique to find functional decomposition. With Jon T. Butler, Sasao also developed the concept of bi-decompsition [64]. This technique is promising for fast minimization of SOPs [2, 14, 23].

# 6 Cascade Realization

Like the PLA, a cascade has a regular structure, and is easier to design than random logic networks [9, 12, 19, 143].

Sasao found an efficient method to map a logic function represented by a BDD into a cascade of lookup tables (or LUT cascade). He also invented a method to realize multiple-output logic function using a large (LUT) and a sequencer [25, 27].

# 7 Complexity Issue of Logic Networks

Sasao made some contributions to the understanding of the complexity of logic circuits. In [118, 126, 139], he presented a method to estimate the average size of PLA's. With Jon T. Butler, Sasao analyzed the maximal numbers of products in irredundant sum-of-products expressions [28]. This shows that a heuristic minimization algorithm sometimes obtains SOPs with many more products than exact minimum SOPs.

As for logic networks with EXOR gates, he derived numbers of products in AND-EXOR expressions for various classes of functions [68, 120].

# 8 Design of Three-Level Networks

## 8.1 OR-AND-OR three-level networks

Sasao has developed a method to realize logic functions by OR-AND-OR three-level networks under the condition that both true and complemented variables are available, and each gate has no fan-in and fan-out constraints. He also considered the number of gates to realize logic functions [79, 123].

## 8.2 AND-OR-EXOR three-level networks

Sasao considered design methods for AND-OR-EXOR three-level networks, where single two-input EXOR gate is used for each output. The network realizes an EXOR of two sum-of-products expressions (EX-SOP), $F_1 \oplus F_2$, where $F_1$ and $F_2$ are sum-of-products expressions (SOPs). The problem is to minimize the total number of different products in $F_1$ and $F_2$ [90]. With D. Debnath, Sasao extended the result [34, 54, 61, 70].

# 9 Easily Testable Design

Sasao developed a new method to test AND-EXOR type PLA [67]. With Y. Iguchi, Sasao also found a new method to test RAM using Walsh spectrum [1]. With H. Fujiwara, Sasao developed an easily testable sequential machine [148].

# 10 FPGA Design

Field programmable gate arrays (FPGAs) are devices that can be programmed by the user to implement a logic function. Because of their short turnaround time, they are important for rapid prototyping. Sasao developed a method to design LUT type FPGAs by decision diagrams [99].

## 11 Spectral Analysis of Logic Functions

With R. Stankovic and C. Moraga, Sasao showed that an original function and its spectram transform can be represented by an EXOR-based decision diagram [85].

## 12 Other Topics

Sasao invented various methods to represent symmetric functions [40, 56, 63]. He also published textbooks on logic design and switching thoery [88, 79, 52, 31]. With Y. Iguchi, Sasao developed logic simulators [42, 39, 35]. With Jon. T. Butler, he has shown that multiple-valued combinational circuits require feedback to minimize the number of gates [98].

## 13 Textbooks Refereeing Sasao's Work

Sasao's fundamental contributions on logic design are included in the following textbooks [160, 159, 158, 157, 156, 155, 154, 152, 151, 153, 150, 149].

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