Programmable Logic Device with an 8-stage cascade of 64K-bit Asynchronous SRAMs

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Outline

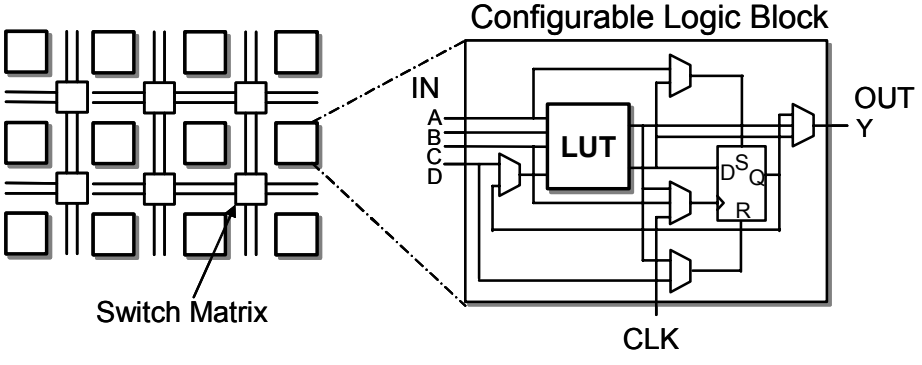
- Background
- LUT-cascade Chip Implementation
  - Structure of LUT Cascade LSI
  - Structure of LUT Block
  - Measurement Result
- Performance Comparison with FPGA
- Summary

Background

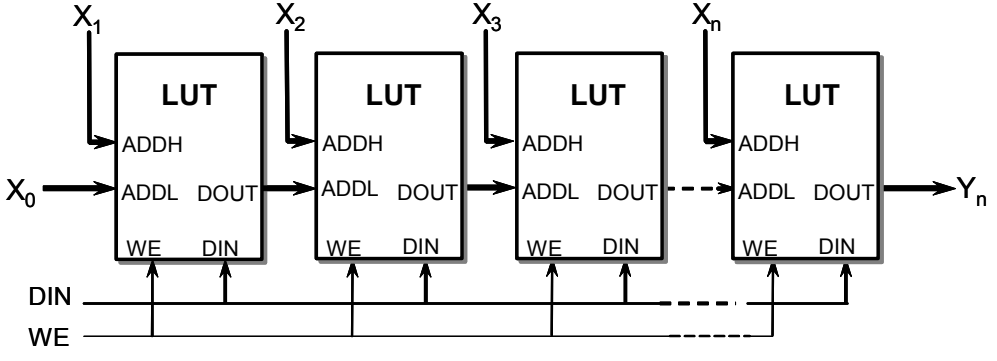
- LUT (Look-Up Table)-cascade[1] was proposed as a new programmable logic architecture
  - Memory-base and simple structure
- LUT-cascade has not been implemented in Chip
  - Speed, Area and Power was not examined in Silicon
- We developed the first implementation of an LSI using LUT-cascade architecture in 0.35um Standard CMOS logic process.

[1] Y.Iguchi, T.Sasao, and M.Matsuura, "Realization of multiple-output functions by reconfigurable cascades", International Conference on Computer Design (ICCD2001), Sep.2001, pp388-393.

Comparison of Programmable Logic Architecture

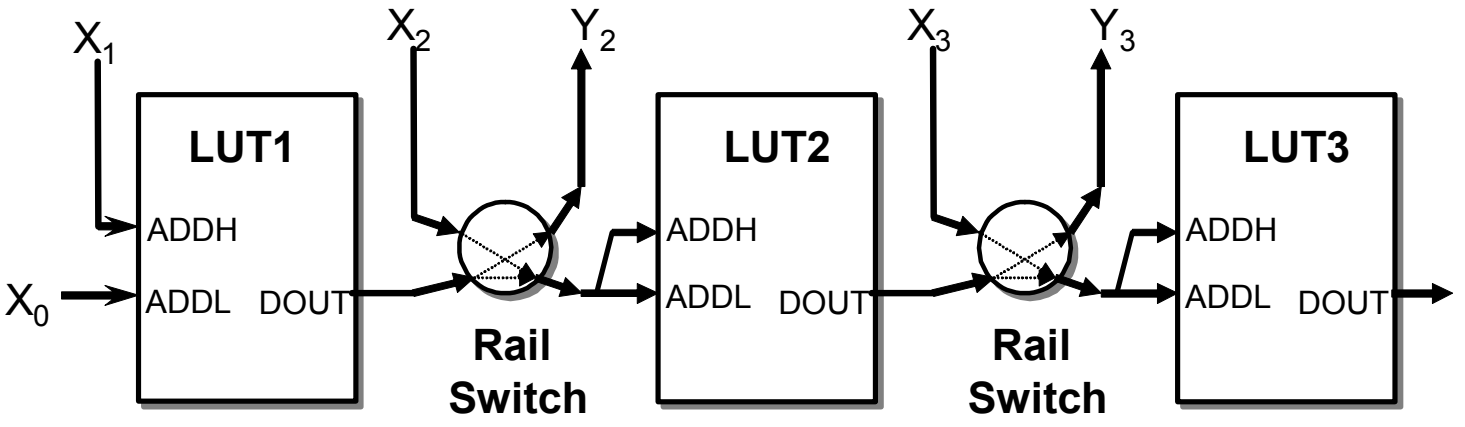


(1) FPGA (LUT Size : 16 - 64bit)

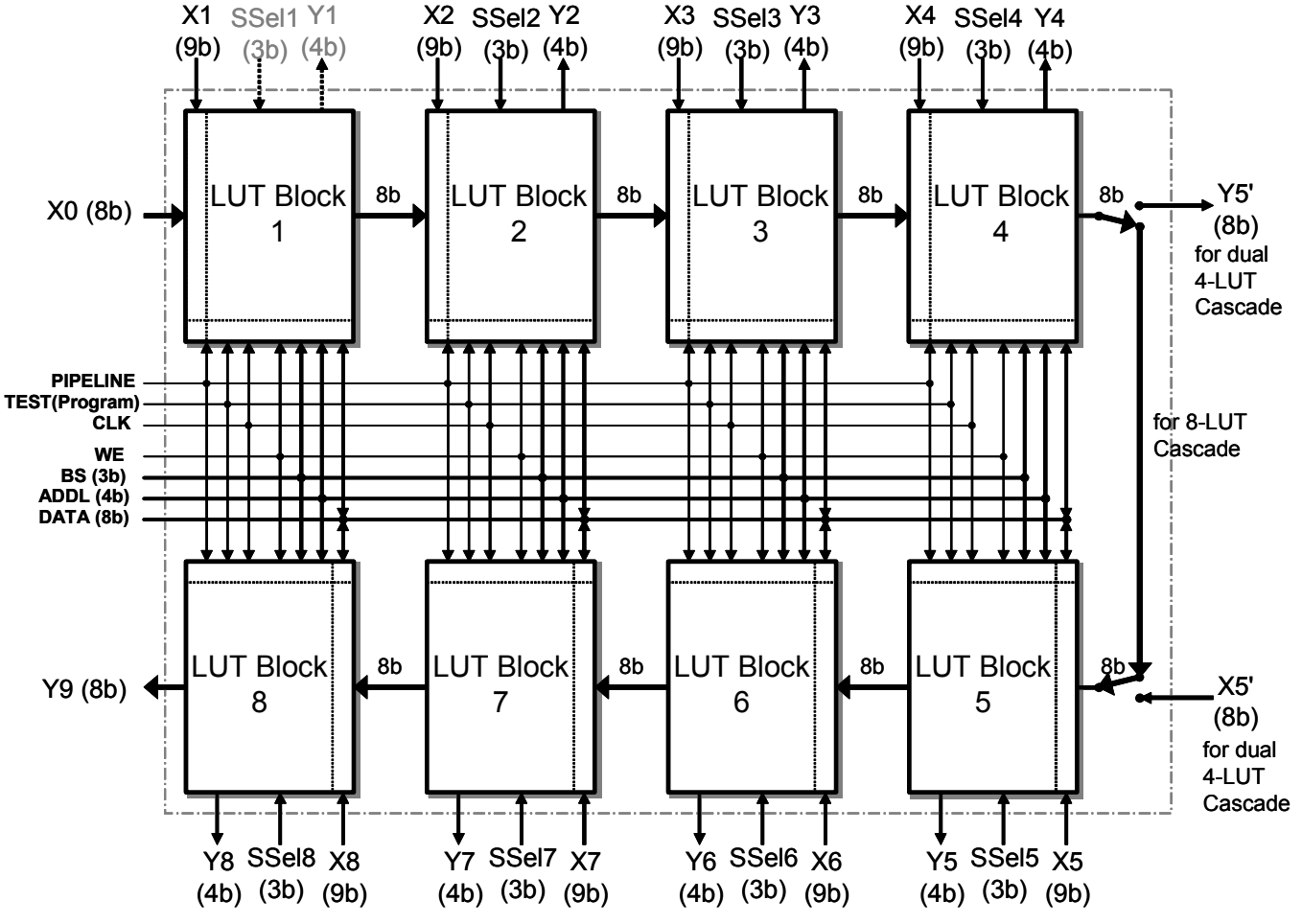


(2) LUT Cascade （LUT Size : 1K - 1Mbit）

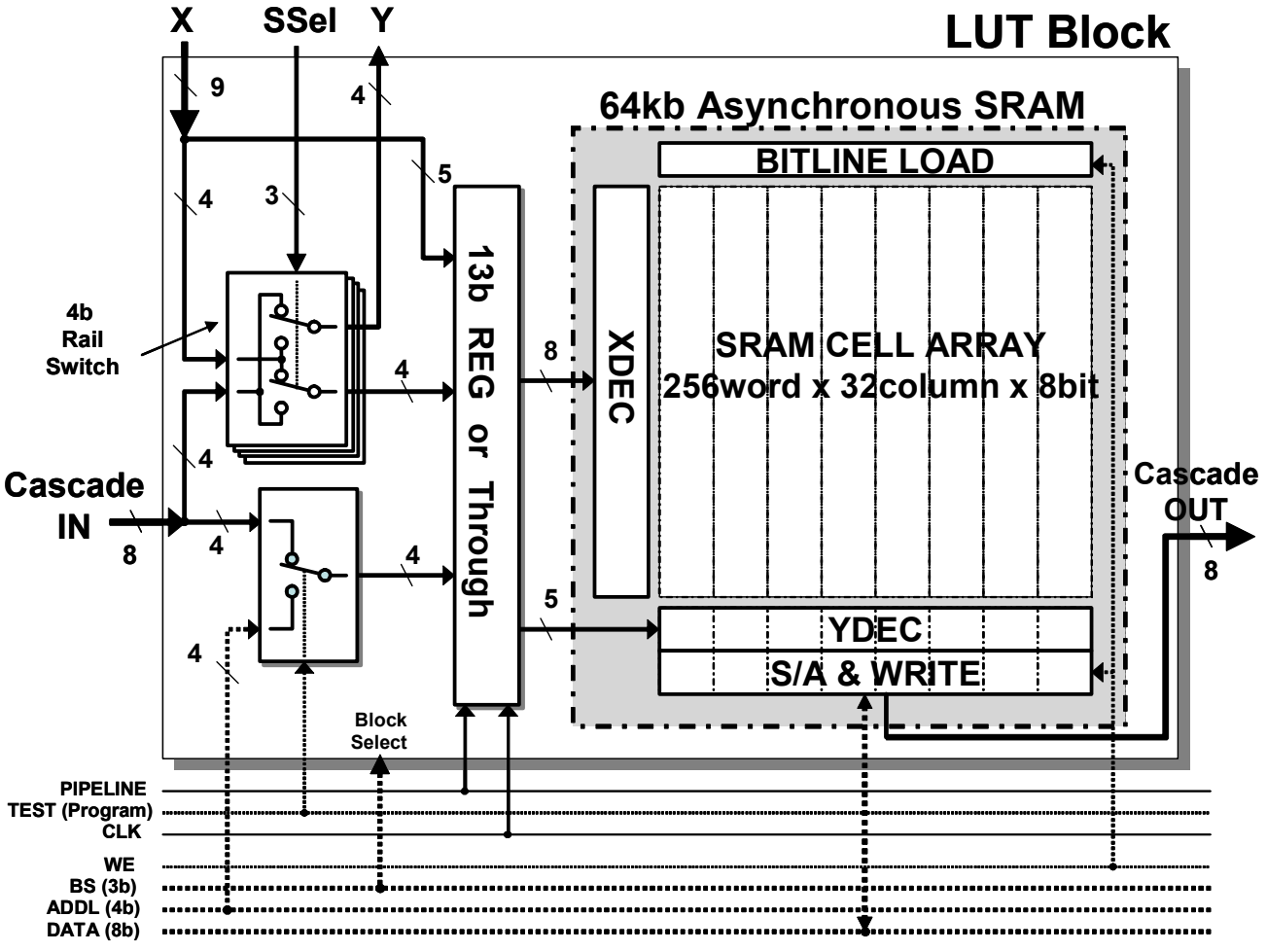
LUT Cascade with Rail Switches



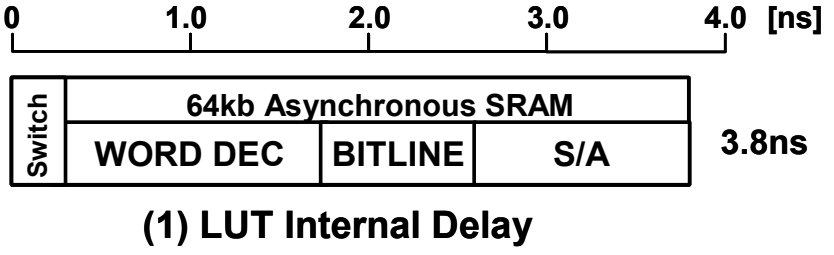
Block Diagram of LUT Cascade LSI



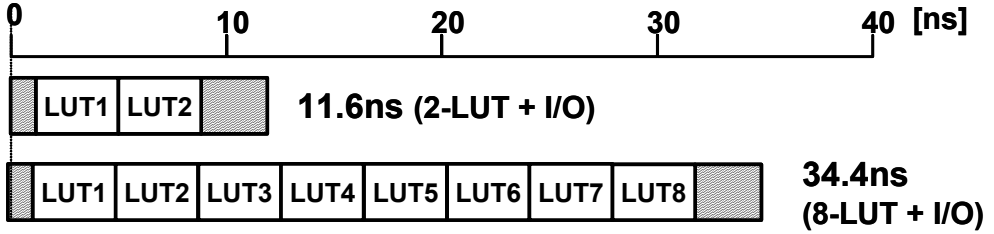
Look-Up Table (LUT) Block



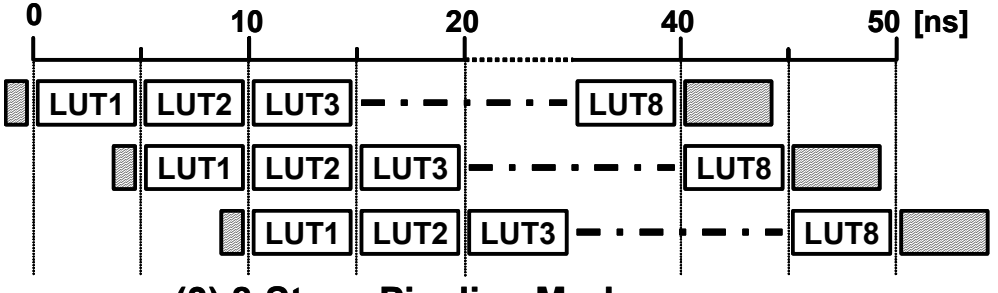
Delay Time Distribution



(1) LUT Internal Delay

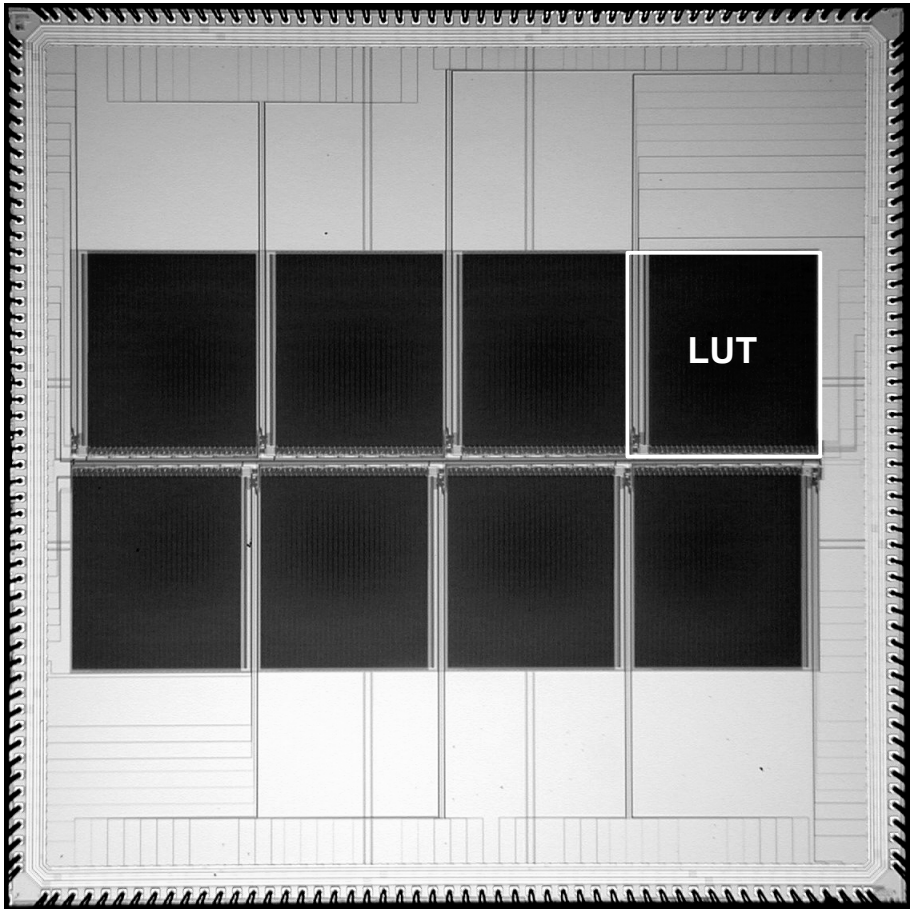


(2) Asynchronous Cascade Delay



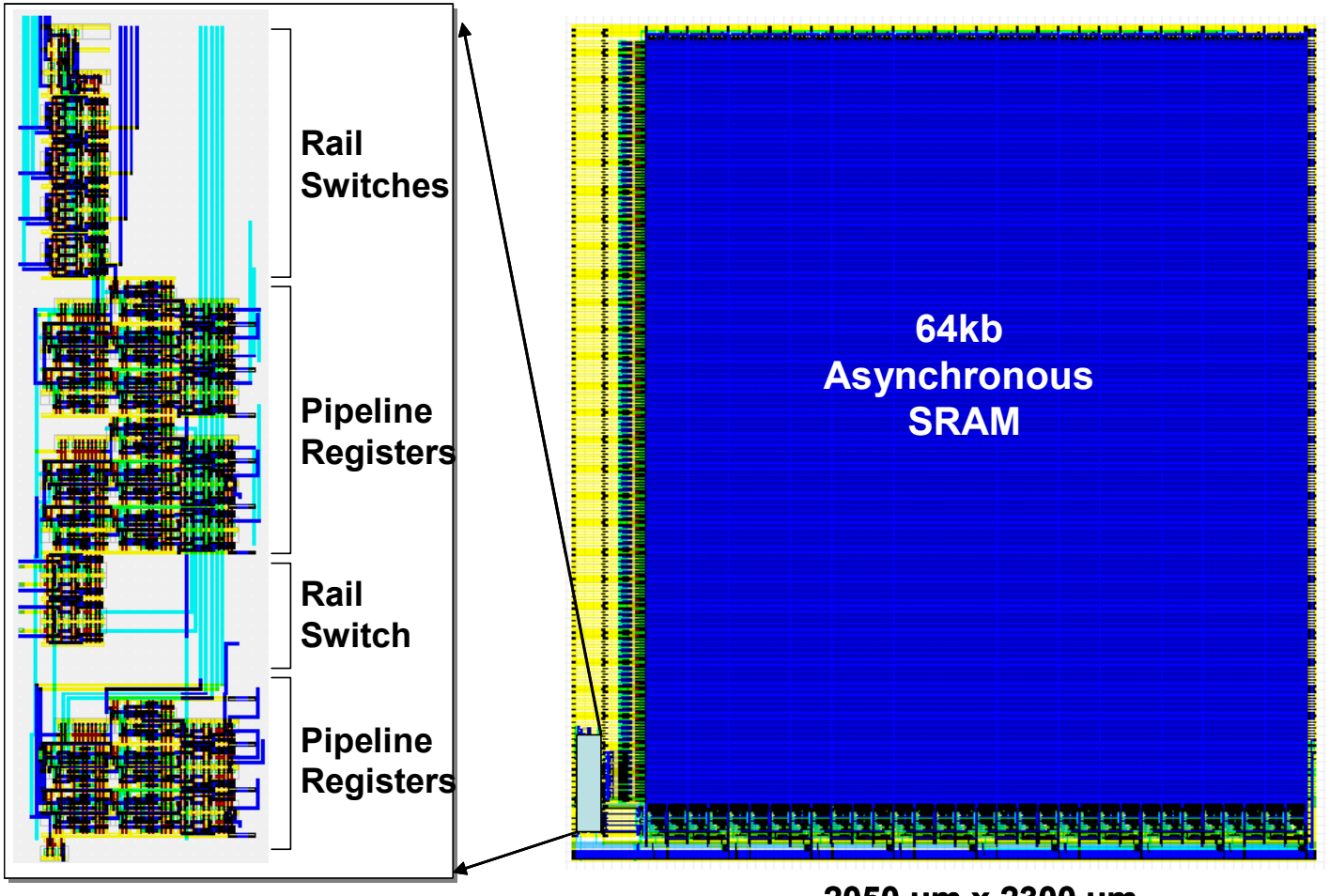
(3) 8-Stage Pipeline Mode

Chip Photomicrograph

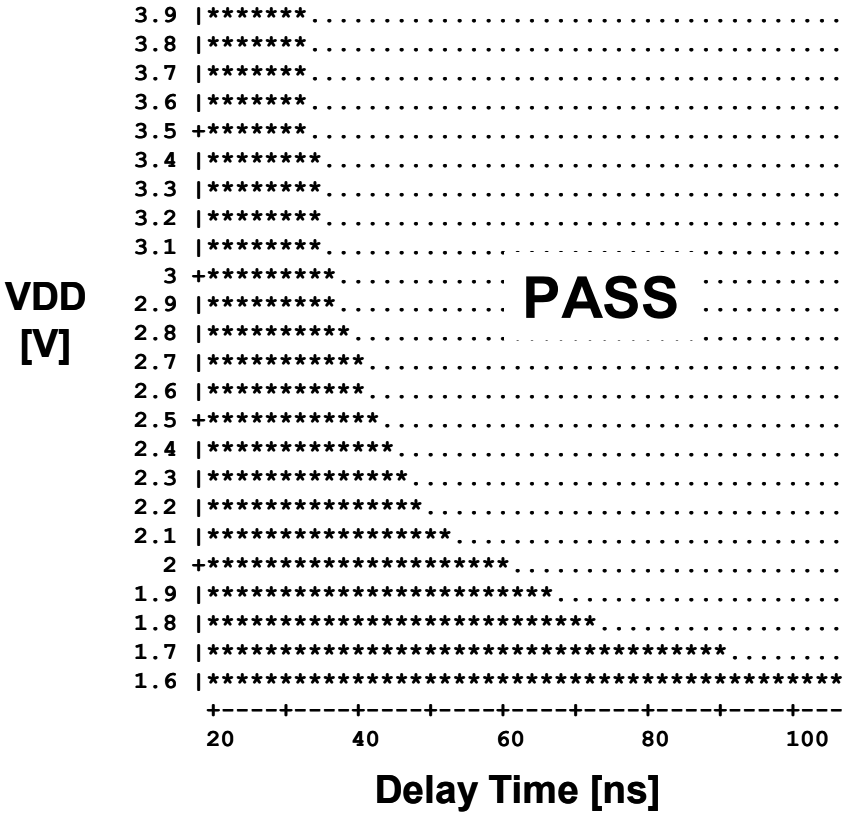


(Core Size : 4.6mm x 8.2mm, Chip Size : 9.8mm x 9.8mm, 208pins)

Layout of LUT Block



Measured Shmoo Plot



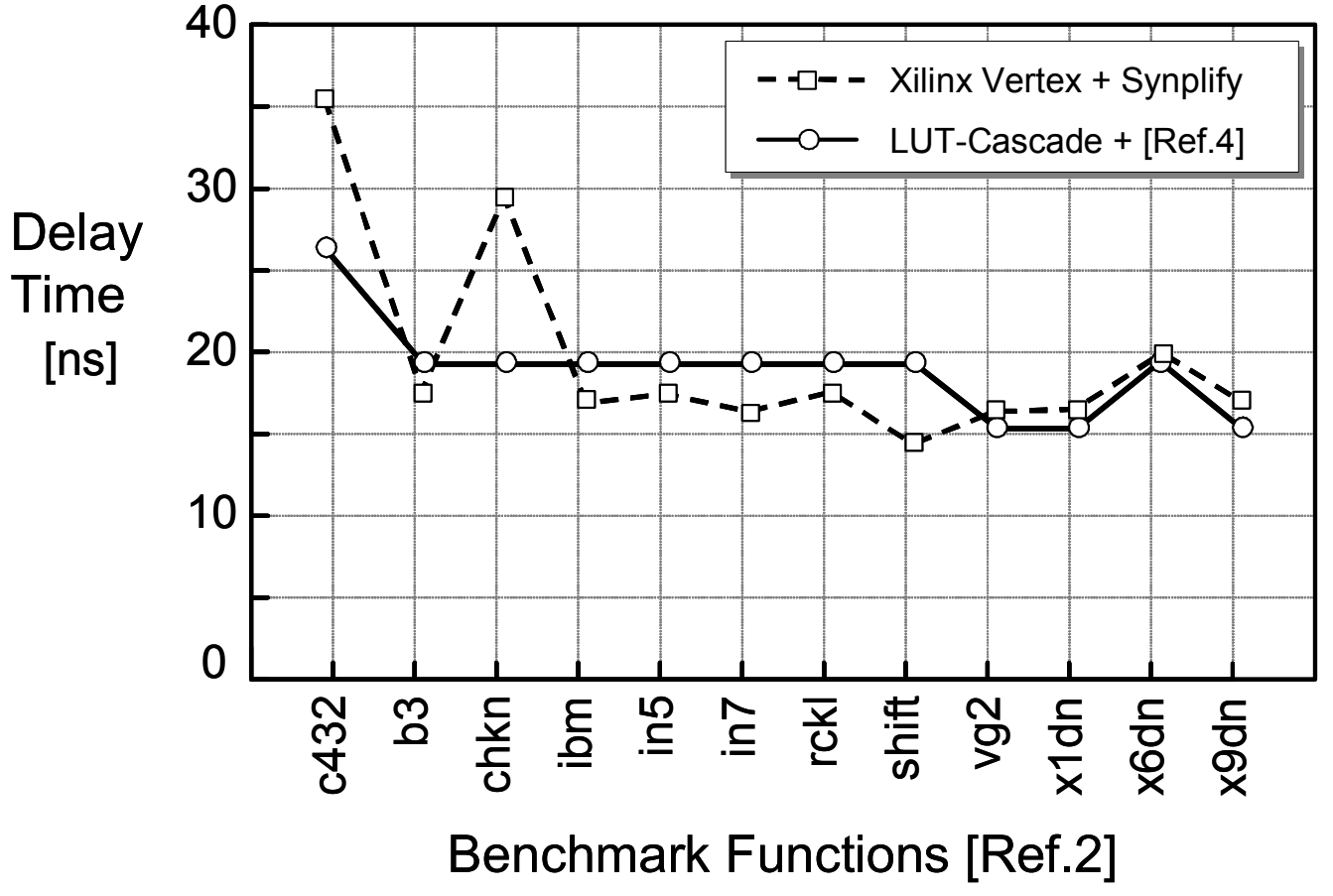
Chip Features

Process Technology	**0.35-um 3-Metal Standard CMOS**
Cascade Configuration	**8-LUT cascade or dual 4-LUT cascade**
Core Area	**4.6 mm x 8.2 mm (8 LUTs)**
LUT Size	**64kbit (8Kw x 8bit)**
Memory Cell	**6-Tr SRAM (6.1 um x 8.25 um)**
Operating Speed	**34.4ns (Asynchronous 8-LUT cascade) 200MHz (Pipeline mode)**
Power	**1.38W (8-LUT Pipeline @ 200MHz)**

Experimental Result of Function Mapping

Target Function [2]	No. of inputs	No. of Outputs	LUT Cascade (0.35um CMOS, 3.3V)				FPGA (0.22um CMOS, 2.5V) [3]			
			No. of LUTs	Area [mm^2]	Delay [ns]	Power [mW / 20MHz]	No of CLBs	Area [mm^2]	Delay [ns]	Power [mW / 20MHz]
C432	36	7	6	28.3	26.8	103.5	98	7.7	35.6	56.7
b3	32	20	4	18.9	19.2	69.0	125	9.8	17.3	63.6
chkn	29	7	4	18.9	19.2	69.0	121	9.5	29.1	66.1
ibm	48	17	4	18.9	19.2	69.0	95	7.4	17.2	62.3
in5	24	14	4	18.9	19.2	69.0	118	9.2	18.2	52.0
in7	26	10	4	18.9	19.2	69.0	73	5.7	16.8	46.9
rckl	32	7	4	18.9	19.2	69.0	94	7.3	18.0	53.3
shift	19	16	4	18.9	19.2	69.0	76	5.9	14.8	52.2
vg2	25	8	3	14.1	15.4	51.2	69	5.4	16.2	46.8
x1dn	27	6	3	14.1	15.4	51.2	66	5.2	16.1	45.0
x6dn	39	5	4	18.9	19.2	69.0	119	9.3	19.7	67.5
x9dn	27	7	3	14.1	15.4	51.2	69	5.4	17.2	46.9
Ave.	30.3	10.3	3.9	**18.5**	**18.9**	**67.6**	93.6	**7.3**	**19.7**	**54.9**

Delay Time Comparison of Function Mapping



Summary

- The first LUT-cascade LSI was developed with eight 64K-bit asynchronous SRAMs in 0.35um Standard CMOS logic process.
  - This chip operates in an 8-stage pipeline mode with 200MHz, or an asynchronous mode with a latency of 34.4ns.
  - The additional hardware to make the memory into cascade is very small: it adds 0.4% to the area, and 0.2% to the transistor counts
- Benchmark results show that it has a comparable performance to FPGAs.
  - By using the same process technology as the FPGA for the LUT cascade, we can achieve a comparable layout area with less delay time and less power dissipation.

References

[1] Y.Iguchi, T.Sasao, and M.Matsuura, "Realization of multiple-output functions by reconfigurable cascades", International Conference on Computer Design (ICCD2001), Sep.2001, pp388-393.

[2] MCNC-benchmark functions: http: //www.cbl.ncsu.edu /www/

[3] http://www.xilinx.com/

[4] T.Sasao and M.Matsuura, "A method to decompose multiple-output circuits by using binary decision diagrams", Proc. of 41th Design Automation Conference, Jun. 2004, pp.428-433.

[5] R. K. Brayton, “The future of logic synthesis and verification,” in Soha and Sasao (eds.), Logic Synthesis and Verification, Kluwer, Nov. 2001.