

# ISMVL 2016

May 18 – 20, 2016, Hokkaido University, Sapporo, Japan

## Final Program



Sponsored by:



IEEE Computer Society



TC on Multiple-Valued Logic

Japan Research  
Group of MVLNational Institute of Information  
and Communications Technology

### May 17, Tuesday

10:00	Post-Binary ULSI Workshop Workshop Chair: <i>H. Nakahara</i>	Room: Seminar Room 1
18:00	ISMVL Welcome Reception (ULSI WS Student Poster Session)	Kogakubu Syokudo (Cafeteria)

### May 18, Wednesday

09:00	Opening Symposium Chair: <i>T. Hanyu</i> and Program Chair: <i>Y. Yuminaka</i>		Room: Akira Suzuki Hall (ASH)
09:15	<b>[Keynote Address I]</b> Chair: <i>T. Hanyu</i> <b>Elucidation of Brain Activities by Electroencephalograms and its Application to Brain Computer Interface</b> <i>Takahiro Yamanoi (Hokkai-Gakuen University, Japan)</i>		Room: ASH
10:00	Coffee/Tea Break		Entrance Hall
	<b>[Session 1A: Circuits I]</b> Chair: <i>M. Natsui</i>	<b>[Session 1B: Synthesis of Reversible Circuits]</b> Chair: <i>R. Wille</i>	Room: ASH Room: Seminar Room 2 (SR2)
10:20	<b>Energy-Efficient and Highly-Reliable Nonvolatile FPGA Using Self-Terminated Power-Gating Scheme</b> <i>D. Suzuki and T. Hanyu</i>	<b>Re-writing HDL Descriptions for Line-aware Synthesis of Reversible Circuits</b> <i>Z. Alwardi, R. Wille, and R. Drechsler</i>	
10:45	<b>CNTFET-RFB: An Error Correction Implementation For Multi-Valued CNTFET Logic</b> <i>G. Sundararajan and C. Winstead</i>	<b>An Improved Factorization Approach to Reversible Circuit Synthesis Based on EXORs of Products of EXORs</b> <i>L. Tran, A. Gronquist, M. Perkowski, and J. Caughman</i>	
11:10	<b>Ternary versus Binary Multiplication with Current-Mode CNTFET-based K-Valued Converters</b> <i>M. Moradi, R. F. Mirzaee, and K. Navi</i>	<b>Fault Detection in Parity Preserving Reversible Circuits</b> <i>N. Przigoda, G. Dueck, R. Wille, and R. Drechsler</i>	
11:35	<b>Design of Ratioless Ternary Inverter using Graphene Barristor</b> <i>C.-H. Shim, S. Heo, J. Noh, Y. J. Kim, S.-Y. Kim, A. K. Khan, and B. H. Lee</i>	<b>Notes on Majority Boolean Algebra</b> <i>A. Chattopadhyay, L. Amaru, M. Soeken, P.-E. Gaillardon, and G. De Micheli</i>	
12:00	Lunch (Symposium Subcommittee Meeting)		Hokubu Shokudo (Cafeteria)

May 18, Wednesday (continued)		
13:20	<b>[Keynote Address II]</b> Chair: <i>M. F. Kawaguchi</i> Room: ASH <b>Realization of Associative Image Search: Development of Image Retrieval Platform for Enhancing Serendipity</b> <i>Miki Haseyama (Hokkaido University, Japan)</i>	
14:05	Coffee/Tea Break Entrance Hall	
	<b>[Session 2A: Circuits II]</b> Chair: <i>N. Homma</i> Room: ASH	<b>[Session 2B: Clone]</b> Chair: <i>D. Simovici</i> Room: SR2
14:20	<b>An FFT Circuit Using Nested RNS in a Digital Spectrometer for a Radio Telescope</b> <i>H. Nakahara, T. Sasao, H. Nakanishi, K. Iwai, T. Nagao, and N. Ogawa</i>	<b>Monomial Clones: Local Results and Global Properties</b> <i>H. Machida and J. Pantovic</i>
14:45	<b>Double-Rate Equalization Using Tomlinson-Harashima Precoding for Multi-Valued Data Transmission</b> <i>Y. Iijima and Y. Yuminaka</i>	<b>Centralizing Monoids on a Three-Element Set Related to Binary Idempotent Functions</b> <i>H. Machida and I. G. Rosenberg</i>
15:10	<b>Context-Based Error Correction Scheme Using Recurrent Neural Network for Resilient and Efficient Intra-Chip Data Transmission</b> <i>N. Sugaya, M. Natsui, and T. Hanyu</i>	<b>Minimal Weighted Clones with Boolean Support</b> <i>P. G. Jeavons, A. Vaicenavicius, and S. Zivny</i>
15:35	Coffee/Tea Break Entrance Hall	
	<b>[Session 3A: Index Generation Functions]</b> Chair: <i>Y. Iguchi</i> Room: ASH	<b>[Session 3B: Algebra I]</b> Chair: <i>F. Manyá</i> Room: SR2
15:50	<b>An Efficient Heuristic for Linear Decomposition of Index Generation Functions</b> <i>S. Nagayama, T. Sasao, and J. T. Butler</i>	<b>Set Representation of Partial Dynamic De Morgan Algebras</b> <i>I. Chajda and J. Paseka</i>
16:15	<b>Index Generation Functions based on Linear and Polynomial Transformations</b> <i>H. Astola, R. Stankovic, and J. Astola</i>	<b>Tolerance Distances on Minimal Coverings</b> <i>C. Zara and D. A. Simovici</i>
16:40	<b>An Algebraic Approach to Reducing the Number of Variables of Incompletely Defined Discrete Functions</b> <i>J. Astola, P. Astola, R. Stankovic, and I. Tabus</i>	<b>Paraconsistent Double Negation That Can Simulate Classical Negation</b> <i>Norihiro Kamide</i>
17:05	<b>A Realization of Index Generation Functions Using Multiple IGUs</b> <i>T. Sasao</i>	<b>Cut-Free Systems for Restricted Bi-Intuitionistic Logic and Its Connexive Extension</b> <i>Norihiro Kamide</i>

May 19, Thursday		
09:15	<b>[Keynote Address III]</b> Chair: <i>T. Sasao</i> Room: ASH <b>Power of Enumeration --- BDD/ZDD-Based Techniques for Discrete Structure Manipulation</b> <i>Shin-ichi Minato (Hokkaido University, Japan)</i>	
10:00	Coffee/Tea Break Entrance Hall	
	<b>[Session 4A: From Reversible to Quantum Circuits]</b> Chair: <i>M. Lukac</i> Room: ASH	<b>[Session 4B: Algebra II]</b> Chair: <i>J. Paseka</i> Room: SR2
10:20	<b>Integrated Synthesis of Linear Nearest Neighbor Ancilla-Free MCT Circuits</b> <i>M. M. Rahman, G. W. Dueck, A. Chattopadhyay, and R. Wille</i>	<b>Some Properties of Generalized State Operators on Residuated Lattices</b> <i>M. Kondo and M. F. Kawaguchi</i>
10:45	<b>Technology Mapping of Reversible Circuits to Clifford+T Quantum Circuits</b> <i>N. Abdessaied, M. Amy, M. Soeken, and R. Drechsler</i>	<b>Simple Characterizations of Perfect Residuated Lattices</b> <i>M. Kondo</i>

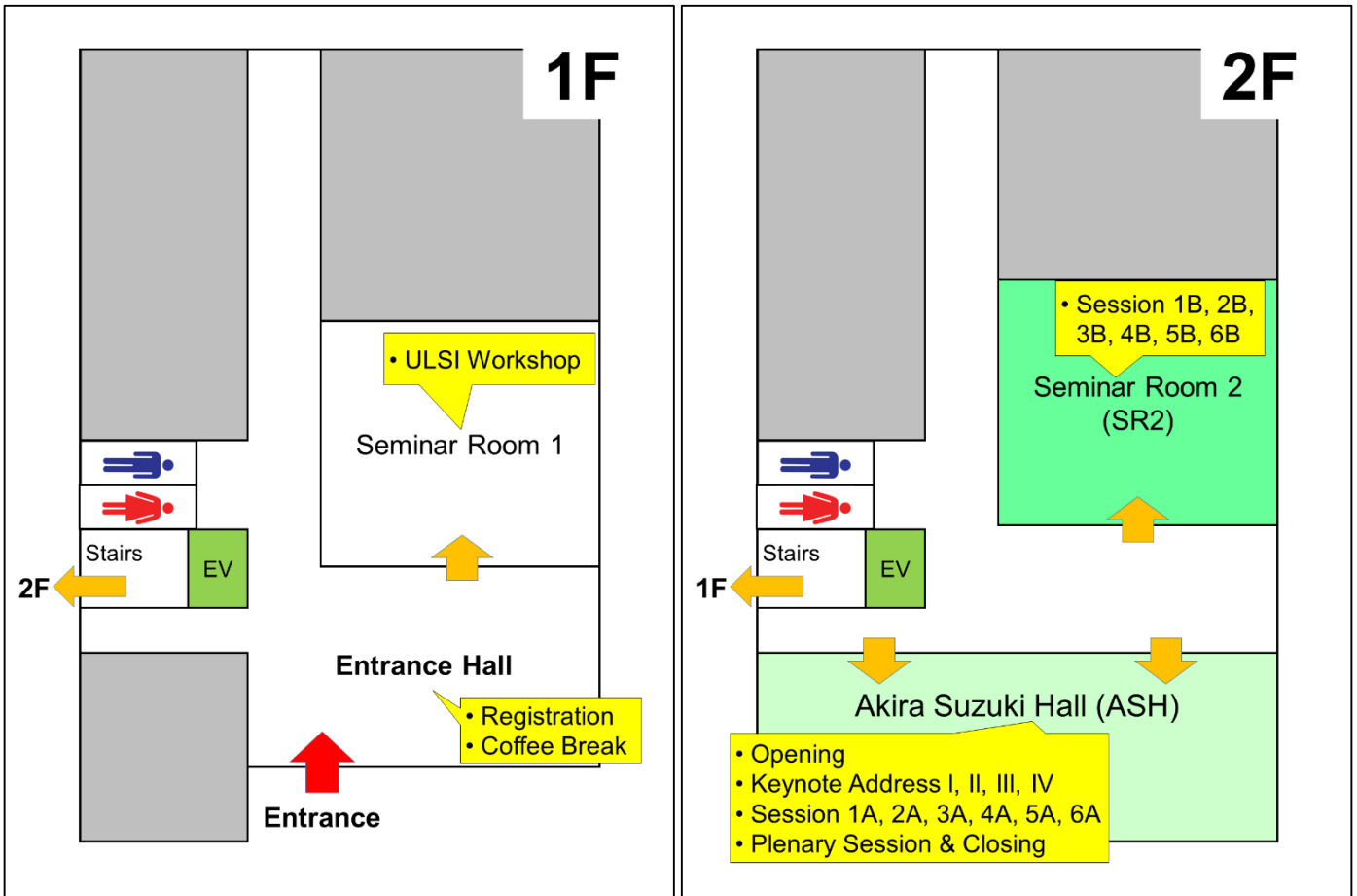
**May 19, Thursday (continued)**

11:10	<b>Nearest-Neighbor and Fault-Tolerant Quantum Circuit Implementation</b> <i>L. Biswal, C. Bandyopadhyay, A. Chattopadhyay, R. Wille, R. Drechsler, and H. Rahaman</i>	
11:40	Lunch, Excursion to NIKKA WHISKY & Otaru Canal, and Banquet at Keio Plaza Hotel Sapporo	

**May 20, Friday**

09:15	<b>[Keynote Address IV] Chair: Y. Yuminaka</b> <b>SPRUCE, an Embedded Compact Stack Machine for IGBT Power Modules</b> <i>Wai Tung Ng and Andrew Shorten (University of Toronto, Canada)</i>		<b>Room: ASH</b>
10:00	Coffee/Tea Break		<b>Entrance Hall</b>
	<b>[Session 5A: Intelligent Medical and Welfare Engineering]</b> Chair: <i>T. Araki</i>	<b>[Session 5B: Logic I]</b> Chair: <i>S. Nagayama</i>	<b>Room: ASH</b>  <b>Room: SR2</b>
10:15	<b>Gray-Scale Morphology Based Image Segmentation and Character Extraction Using SVM</b> <i>J. Chen and N. Takagi</i>	<b>Gibbs Characterization of Binary and Ternary Bent Functions</b> <i>R. S. Stankovic, M. Stankovic, J. T. Astola, and C. Moraga</i>	
10:40	<b>A Low-Voltage and Low-Power CMOS Temperature Sensor Circuit with Digital Output for Wireless Healthcare Monitoring System</b> <i>A. Setiabudi, R. Sakamoto, H. Tamura, and K. Tanno</i>	<b>On Constructing Secure and Hardware-Efficient Invertible Mappings</b> <i>E. Dubrova</i>	
11:05	<b>Dependency Analysis of BMI in Health Checkup Blood Data</b> <i>M. Higuchi, K. Sorachi, and Y. Hata</i>	<b>Formal Design of Pipelined GF Arithmetic Circuits and Its Application to Cryptographic Processors</b> <i>R. Ueno, Y. Sugawara, N. Homma, and T. Aoki</i>	
11:30	<b>Novel Instrumentation Amplifier Architectures Insensitive to Resistor Mismatches and Offset Voltage for Biological Signal Processing</b> <i>Z. Abidin, K. Tanno, S. Mago, and H. Tamura</i>	<b>Realization of FIR Digital Filters Based on Stochastic/Binary Hybrid Computation</b> <i>S. Koshita, N. Onizawa, M. Abe, T. Hanyu, and M. Kawamata</i>	
11:55	<b>Study Support System of Character Drawing considering Feeling Evaluation</b> <i>R. Murakami and N. Muranaka</i>	<b>The Pascal triangle (1654), the Reed-Muller-Fourier Transform (1992), and the Discrete Pascal Transform (2005)</b> <i>C. Moraga, R. Stankovic, and M. Stankovic</i>	
12:20	Lunch (Executive Subcommittee Meeting)		<b>Hokubu Shokudo (Cafeteria)</b>
	<b>[Session 6A: Quantum Gates and Quantum States]</b> Chair: <i>G. Dueck</i>	<b>[Session 6B: Logic II]</b> Chair: <i>R. Stankovic</i>	<b>Room: ASH</b>  <b>Room: SR2</b>
13:40	<b>New Two-Qubit Gate Library with Entanglement</b> <i>M. B. Ali, T. Hirayama, K. Yamanaka, and Y. Nishitani</i>	<b>A Study on Realizing Awareness Using 3VL-MLP</b> <i>Q. Zhao</i>	
14:05	<b>Quantum p-Valued Toffoli and Deutsch Gates with Conjunctive or Disjunctive Mixed Polarity Control</b> <i>C. Moraga</i>	<b>Multi-Valued Problem Solvers</b> <i>B. Steinbach, S. Heinrich, and C. Posthoff</i>	
14:30	<b>Logic Synthesis for Quantum State Generation</b> <i>P. Niemann, R. Datta, and R. Wille</i>	<b>A Bit-Vector Approach to Satisfiability Testing in Finitely-Valued Logics</b> <i>J. R. Soler and F. Manyà</i>	
14:55	<b>Quantum Algorithmic Complexity of Three-Qubit Pure States</b> <i>M. Lukac and A. Mandilara</i>	<b>On the Inadmissible Class of Multiple-Valued Faulty-Functions under Stuck-at Faults</b> <i>D. Chowdhury, D. K. Das, B. B. Bhattacharya, and T. Sasao</i>	
15:20	Coffee/Tea Break		<b>Entrance Hall</b>
15:30	Plenary Session and Closing		<b>Room: ASH</b>

# Brief Map of the Building



# Brief Map for Reception & Lunch (Outside the Building)

