ISMVL-2013
IEEE 43rd International Symposium on Multiple-Valued Logic
Toyama International Conference Center, Toyama, Japan, May 21 – 24

Sponsored by: IEEE computer society (IEEE Computer Society); TC on Multiple-Valued Logic; Japan MVL Research Group

FINAL PROGRAM

May 21, Tuesday		
09:00	Post-Binary ULSI Workshop Registration	**2F Foyer**
09:40	**[Post-Binary ULSI Workshop Invited Talk]** **Room 201** **Ultrahigh-Speed Digital-to-Analog Converters for Multi-Level Optical Transmission Systems** *Munehiko Nagatani, Hideyuki Nosaka, Shogo Yamanaka, and Koichi Murata (NTT Photonics Lab., Japan)*	
10:55	Post-Binary ULSI Workshop Regular Sessions **Room 201** Workshop Co-Chairs: *N. Homma and S. Nagayama*	
17:00	ISMVL Registration	**2F Foyer**
18:00	ISMVL Welcome Reception (ULSI WS Student Poster Session*)	**3F Foyer**

May 22, Wednesday		
08:15	ISMVL Registration	**2F Foyer**
08:45	Opening **Room 201/202** Symposium Chair: *T. Waho* and Program Chair: *Y. Yuminaka*	
09:00	**[Invited Address I*]** Chair: *T. Waho* **Room 201/202** **Computational Medical and Health Care Technology** *Yutaka Hata (University of Hyogo, Japan) and Hiroshi Nakajima (Omron Co., Japan)*	
09:50	Break	
	[Session 1A: Medical and Health Care Engineering] Chair: *N. Kamiura* **Room 201/202**	**[Session 1B: Reversible Circuits]** Chair: *M. Lukac* **Room 203**
10:10	**Systems Health Care – Health Management Technology –** *H. Nakajima, T. Shiga, and Y. Hata*	**Fault Ordering for Automatic Test Pattern Generation of Reversible Circuits** *R. Wille, H. Zhang, and R. Drechsler*
10:35	**Wearable Human Activity Recognition by Electrocardiograph and Accelerometer** *T. Fujimoto, H. Nakajima, N. Tsuchiya, H. Marukawa, K. Kuramoto, S. Kobashi, and Y. Hata*	**Synthesis of Reversible Circuits Based on Exclusive OR Sums** *B. Schaeffer, L. Tran, A. Gronquist, M. Perkowski, and P. Kerntopf*
11:00	**Gaze Estimation Using Electrooculogram Signals and Its Mathematical Modeling** *M. Yan, H. Tamura, and K. Tanno*	**Multiple-Valued Reversible Benchmarks and Extensible Quantum Specification (XQS) Format** *M. Hawash, M. Lukac, M. Kameyama, and M. Perkowski*
11:25	**Fuzzy Damage Extraction Method for Ultrasonic Nondestructive Testing Images** *K. Tsukuda, T. Egawa, K. Taniguchi, K. Kuramoto, S. Kobashi, and Y. Hata*	**Analysis and Improvement of Transformation-Based Reversible Logic Synthesis** *C. Chandak, A. Chattopadhyay, S. Majumder, and S. Maitra*
11:50	Lunch (Symposium Committee)	

May 22, Wednesday (continued)		
	[Session 2A: Medical and Wellness Applications] Chair: *H. Nakajima* **Room 201/202**	**[Session 2B: Logic Design/Switching Theory I]** Chair: *E. Dubrova* **Room 203**
13:00	**A Fuzzy Human Detection for Security System Using Infrared Laser Camera** *T. Takeda, K. Kuramoto, S. Kobashi, and Y. Hata*	**Remarks on Applications of Shapes of Decision Diagrams in Classification of Multiple-Valued Logic Functions** *S. Stanković, R. S. Stanković, and J. Astola*
13:25	**Mining Multi Human Locations Using Thermopile Array Sensors** *M. Kuki, H. Nakajima, N. Tsuchiya, K. Kuramoto, S. Kobashi, and Y. Hata*	**A Machine to Evaluate Decomposed Multi-Terminal Multi-Valued Decision Diagrams for Characteristic Functions** *H. Nakahara, T. Sasao, and M. Matsuura*
13:50	**On Selection of Intraocular Power Formula Using Support Vector Machines and Genetic Algorithm** *N. Kamiura, T. Fukuda, A. Saitoh, T. Isokawa, N. Matsui, and H. Tabuchi*	**An Application of Autocorrelation Functions to Find Linear Decompositions for Incompletely Specified Index Generation Functions** *T. Sasao*
14:15	**A Broken Line Classification Method of Mathematical Graphs for Automating Translation into Scalable Vector Graphic** *N. Takagi and J. Chen*	**A Transfer Function Model for Ternary Switching Logic** *M. A. Thornton*
14:40	**On Synthesis and Verification from Event Diagrams in a Robot Theatre Application** *M. Perkowski, A. Bhutada, M. Lukac, and M. Sunardi*	**Spectral Response of Ternary Logic Netlists** *M. A. Thornton and T. W. Manikas*
15:05	Break	
	[Session 3A: Clone Theory I] Chair: *A. Bulatov* **Room 201/202**	**[Session 3B: Circuits I]** Chair: *K. Tanno* **Room 203**
15:20	**A Study on Essentially Minimal Clones** *H. Machida and I. G. Rosenberg*	**Design and Evaluation of a Differential Switching Gate for Low-Voltage Applications** *M. Natsui, K. Kashiuchi, and T. Hanyu*
15:45	**A Solution to a Problem of D. Lau: Complete Classification of Intervals in the Lattice of Partial Boolean Clones** *M. Couceiro, L. Haddad, K. Schölzel, and T. Waldhauser*	**A Successive Approximation A/D Converter Using Generalized Non-Binary Algorithm** *Y. Kurisu, T. Sasaki, and T. Waho*
16:10	**On the Clones Containing a Near-Unanimity Function** *D. Zhuk and S. Moiseev*	**A Graph-Based Approach to Designing Parallel Multipliers over Galois Fields Based on Normal Basis Representations** *K. Okamoto, N. Homma, and T. Aoki*
16:35	**Intersections with Słupecki Partial Clones on a Finite Set** *L. Haddad and K. Schölzel*	**Low-Power Multiple-Valued Source-Coupled Logic Circuits Using Dual-Supply Voltages for a Reconfigurable VLSI** *X. Bai and M. Kameyama*
17:00	**Not Finitely Definable Partial Clones on a Finite Set** *B. A. Romov*	**Dramatically Low-Transistor-Count High-Speed Ternary Adders** *R. F. Mirzaee, M. H. Moaiyeri, M. Maleknejad, K. Navi, and O. Hashemipour*

May 23, Thursday		
08:45	**[Invited Address II]** Chair: *H. Machida* **Room 201/202** **The Complexity of Łukasiewicz Logic** *Martin Goldstern (Vienna University of Technology, Austria)*	
9:35	Break	
	[Session 4A: Clone Theory II] Chair: *M. Courceiro* **Room 201/202**	**[Session 4B: Algebra and Logic I]** Chair: *N. Takagi* **Room 203**
9:50	**On Hyper Co-Clones** *J. Čolić, H. Machida, and J. Pantović*	**Four Decades of Multi-Valued Logic: Lists of Highly Cited Papers** *T. Sasao*
10:15	**Clones of Partial Cofunctions** *S. Kerkhoff and F. M. Schneider*	**Chaotic Time Series Prediction Using Neuro-Fuzzy Systems with Cluster-Based Tribes Optimization Algorithm** *C.-H. Chen, R.-Z. Jhang, and Y.-Y. Liao*
10:40	**Boolean Max-Co-Clones** *A. A. Bulatov*	**Join Operations on Commutative BCK-Algebras with Condition (S)** *M. F. Kawaguchi, K. Minami, and M. Kondo*
11:10	**[Special Talk*]** Chair: *K. Nakashima* **Room 201/202** **Local Energy Production for Local Consumption Using Micro Hydro Power** *Hiroyuki Uesaka (Toyama University of International Studies, Japan)*	
12:00	Excursion to Gokayama / Zuiryu-ji with lunch	
19:00	Banquet	

May 24, Friday		
08:45	**[Invited Address III]** Chair: *Y. Yuminaka* **Room 201/202** **Highly Reliable Non-Volatile Logic Circuit Technology and Its Application** *H. Kimura, Z. Zhong, Y. Mizuochi, N. Kinouchi, Y. Ichida, and Y. Fujimori (Rohm Co., Ltd., Japan)*	
09:35	Break	
	[Session 5A: Algebra and Logic II] Chair: *T. Araki* **Room 201/202**	**[Session 5B: Circuits II]** Chair: *M. Natsui* **Room 203**
09:50	**Tense Operators and Dynamic De Morgan Algebra** *I. Chajda and J. Paseka*	**Comparing Performance of a Multiple-Valued Time-Based Serial Data Link with Other Serial Links** *M. Rashdan and J. Haslett*
10:15	**On the Combinatorics of Tolerance Relations** *D. A. Simovici*	**Lowering Error Floors in Stochastic Decoding of LDPC Codes Based on Wire-Delay Dependent Asynchronous Updating** *N. Onizawa, W. Gross, T. Hanyu, and V. Gaudet*
10:40	**On Natural Eight-Valued Reasoning** *N. Kamide*	**Expandable MVL Inverter Compatible with Standard CMOS Process and Its Application to MVL Hysteresis Comparator** *A. A. Mannan, K. Tanno, H. Tamura, T. Toyama, and A. Darmawansyah*
11:05	**Embedding-Based Methods for Trilattice Logic** *N. Kamide*	**Accurate and High-Speed Asynchronous Network-on-Chip Simulation Using Physical Wire-Delay Information** *T. Hanyu, Y. Watanabe, and A. Matsumoto*
11:30	**On the Semigroup of Equational Classes of Finite Functions** *J. Almeida, M. Couceiro, and T. Waldhauser*	**An Area-Efficient Multiple-Valued Reconfigurable VLSI Architecture Using an X-Net** *X. Bai and M. Kameyama*
11:55	Lunch (Executive Committee)	

May 24, Friday (continued)		
	[Session 6A: Logic Design/Switching Theory II] Chair: *M. Miller* **Room 201/202**	**[Session 6B: Algebra and Reversible Circuits]** Chair: *G. Dueck* **Room 203**
13:20	**Noise-Tolerant Model of a Ternary Inverter Based on Markov Random Field** *G. Tangim, S. Yanushkevich, S. Kasai, and V. Shmerko*	**Debugging of Reversible Circuits Using πDDs** *L. Tague, M. Soeken, S. Minato, and R. Drechsler*
13:45	**Minimization of the Number of Edges in an EVMDD by Variable Grouping for Fast Analysis of Multi-State Systems** *S. Nagayama, T. Sasao, and J. T. Butler*	**Analysis of Reversible and Quantum Finite State Machines Using Homing, Synchronizing and Distinguishing Input Sequences** *M. Lukac, M. Kameyama, M. Perkowski, and P. Kerntopf*
14:10	**Secure Key Storage Using State Machines** *N. Li, S. S. Mansouri, and E. Dubrova*	**Exact Template Matching Using Boolean Satisfiability** *N. Abdessaied, M. Soeken, R. Wille, and R. Drechsler*
14:35	**The Impact of Address Arithmetic on the GPU Implementation of Fast Algorithms for the Vilenkin-Chrestenson Transform** *D. Gajić and R. S. Stanković*	**Synthesis of Balanced Ternary Reversible Logic Circuit** *B. Mondal, P. Sarkar, P. K. Saha, and S. Chakraborty*
15:00	**Solution of the Last Open Four-Colored Rectangle-Free Grid – An Extremely Complex Multiple-Valued Problem** *B. Steinbach and C. Posthoff*	**Contribution to the Study of Multiple-Valued Bent Functions** *C. Moraga, M. Stanković, R. S. Stanković, and S. Stojković*
15:25	**Ternary Logic Network Justification Using Transfer Matrices** *M. A. Thornton and J. L. Dworak*	**Alternative Proof of Mulholland's Theorem and New Solutions to Mulholland Inequality** *M. Petrik, M. Navara, and P. Sarkoci*
15:50	Break	
16:00	Plenary Session **Room 201/202**	
17:00	Closing **Room 201/202** Symposium Chair: *T. Waho*	
17:00	Reed-Muller Workshop Registration **2F Foyer**	
17:40	**[Reed-Muller Workshop Invited Talk (Open for ISMVL Attendees)]** **Room 201** **Recent Topics on BDD/ZBDD-Based Discrete Structure Manipulation** *Shin-ichi Minato (Hokkaido University, Japan)*	
19:30	Reed-Muller Workshop **Room 201** Workshop Chair: *T. Sasao*	

May 25, Saturday	
8:45	Reed-Muller Workshop **Room 201** Workshop Chair: *T. Sasao*

Sessions marked with * are open to the public.

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