CALL FOR PAPERS

Reed-Muller 2013

http://www.lsi-cad.com/RM

May 24-25 (Sat-Sun), 2013, Toyama Japan

After the International Symposium on Multiple-Valued Logic, May 22-24, 2013, Toyama, Japan.

In this workshop, we consider various types of representations for discrete functions. AND-EXOR based representations that are simpler than standard AND-OR representations. Decision diagrams for synthesis, analyses, and verification. Spectrum transformation to detect the properties of logic functions. The goal of the Reed-Muller 2013 Workshop is to advance the state-of-the-art by providing a setting in which researchers can exchange ideas. Previous workshops sites are Tuusula (Finland) in 2011, Naha (Japan) in 2009, Oslo (Norway) in 2007, Tokyo (Japan) in 2005, Trier (Germany) in 2003, Starkville, Mississippi (USA) in 2001, Victoria (Canada) in 1999, Oxford (UK) in 1997, Chiba (Japan) in 1995, and Hamburg (Germany) in 1993.

Topics include, but are not limited to: Graph-based representations of logic functions: BDD, MDD, BMD, EVBDD, etc; EXOR-based representations; Spectral representation of logic functions; Graph functions, bent functions, and cryptographic applications; Implementation in silicon (FPLDs, FPGAs, ...); Applications, including circuit design, reversible logic, quantum logic, etc; Representations for quantum computing, nano-technology, and molecular scale computing Cryptographically-significant functions.

Authors are invited to submit full papers not exceeding 10 two-column format pages to

Program Chair: Jon T. Butler, Distinguished Professor Department of Electrical and Computer Engineering Naval Postgraduate School, Code EC/Bu Monterey, CA 93943-5121 U.S.A. 831-656-3299 (O) 831-656-2760 (FAX) jon_butler@msn.com

Submissions should be sent by e-mail as an attached PDF (preferred) or postscript file. Please do not submit papers by regular mail or fax.

Important Dates

Extended abstract / draft paper submission: February 1, 2013
Notification of acceptance: March 24, 2013
Camera Ready Paper Due: April 17, 2013
Workshop May 24-25, 2013 (Fri-Sat)

PC Committee: Jon T. Butler; Rolf Drechsler; Gerhard W. Dueck; D. Michael Miller; Marek Perkowski; Tsutomu Sasao; Radomir Stankovic; Bernd Steinbach; and Mitchell A. Thornton

We are **planning to publish a book in 2014** from Morgan and Claypool. Selected authors are asked to revise the paper to form a chapter of the book. Each chapter must be self-contained and easily read. It should contains examples, exercises and their solutions. Chapter authors are asked revise the submitted chapters according to the chapter reviewers comments until they satisfy the specification of the book.

For Further Questions: **General Chair:**: Tsutomu Sasao, Department of Computer Science and Electronics, Kyushu Institute of Technology, Iizuka Japan, sasao@cse.kyutech.ac.jp

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