Tentative Program for the Reed-Muller 2013 Workshop

May 24, 2013 (Friday)

17:00 Registration

17:30 – 17:40 Opening/Welcome

Session 1: 17:40 – 18:30 (Session Chair – T. Sasao)

17:40 – 18:30 (50 mins.) Invited Talk #1: S. Minato "Recent topics on BDD/ZDD-based discrete structure manipulation"

18:30 – 19:30 (60 mins.) Dinner

Session 2: 19:30 – 20:00 (Session Chair – J. Butler)

17:40 – 18:30 (25 mins.) Special Talk #2: T. Sasao "Forty years of logic synthesis"

May 25, 2013 (Saturday)

Session 3: 08:45 – 10:00 (Session Chair – M. Thornton)

08:45 – 09:10 (25 mins.) Talk #3: T. Hirayama, T. Murayama, K. Yamanaka, and Y. Nishitani, "A lower bound on the gate count of Toffoli-based reversible logic circuits"

09:10 – 09:35 (25 mins.) Talk #4: M. Szyprowski and P. Kerntopf, "Recent approaches to optimization issues in synthesis of reversible circuits"

09:35 – 10:00 (25 mins.) Talk #5: J. Burger, C. Teuscher, and M. Perkowski, "Digital logic synthesis for memristors"

10:00 – 10:15 (15 mins.) Break

Session 4: 10:15 – 11:30 (Session Chair – G. Dueck/B. Steinbach)

10:15 – 10:40 (25 mins.) Talk #6: D. Strukov, A. Mishchenko, and R. Brayton, "Maximum throughput logic synthesis for stateful logic: A case study"

10:40 – 11:05 (25 mins.) Talk #7: S. Nagayama, "Efficient regular expression matching method using ZBDDs"

11:05 – 11:30 (25 mins.) Talk #8: C. Moraga, M. Stankovic, R. Stankovic, and S. Stojkovic, "On multiple-valued hyper-bent functions"

11:30 – 12:30 (60 mins.) Lunch

Session 5: 12:30 – 14:00 (Session Chair –C. Moraga) - 5 minute introduction followed by the poster session (Coffee and refreshments served).

Poster #1: T. Manikas, M. Thornton, and F. Chang, "Mission planning analysis using decision diagrams"

Poster #2: J. Butler and T. Sasao, "Combinatorial computing – One object per clock"

Poster #3: M. Rahman and G. Dueck, "Template matching in quantum circuits optimization"

Poster #4: M. Stankovic and R. Stankovic, "Variable reduction of index generation functions in Walsh-Hadamard domain"

Poster #5: M. Hawash and M. Perkowski, "Generalized multiple-valued swivel gate"

Poster #6: A. Raghuvanshi and M. Perkowski, "Synthesis of incompletely specified logic functions with memristor-realized material implication gates"

Session 6: 14:00 – 14:45 (Session Chair – P. Kerntopf)

14:00 – 14:45 (25 mins.) Talk #9: R. Stankovic, J. Astola, and C. Moraga, "Pascal matrices, Reed-Muller expressions and Reed-Muller error correcting codes"

14:45 – 15:10 (25 mins.) Talk #10: B. Steinbach and C. Posthoff, "Derivative operations for lattices of Boolean functions"

15:10 – 15:35 (25 mins.) Talk #11: K. Datta, G. Rathi, I. Sengupta, and H. Rahaman, "An improved reversible circuit synthesis approach using clustering of ESOP cubes"

Session 7: 15:35 – 16:00 Future of the Workshop (Session Chair – T. Sasao)

16:00 Close